BASE TRANSPORT AND VERTICAL PROFILE ENGINEERING IN $Si/Si_{1-x}Ge_x/Si$ HETEROJUNCTION BIPOLAR TRANSISTORS

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For my parents, Annemarie and Georg Prinz

"Rund ist die Welt, drum Brüder laßt uns reisen "

(The world is round, so let's travel, brothers ...)

Abstract

Recent advances in low-temperature epitaxial growth of strained silicon-germanium alloys on silicon substrates allow bandgap engineering in silicon-based devices, with profound consequences for device design.

In this thesis the improved control by Rapid Thermal Chemical Vapor Deposition of the vertical profile of a $Si/Si_{1-x}Ge_x/Si$ heterojunction bipolar transistor (HBT) is used to study the effect of the shape of the conduction band in the base on device performance.

Near-ideal base currents in $Si/Si_{1-x}Ge_x/Si$ HBT's, limited by hole injection into the emitter, are achieved using a non-ultra-high vacuum (UHV) technique for the first time, proving that high-lifetime $Si_{1-x}Ge_x$ material can be fabricated using processes compatible with standard silicon technology.

Graded-base $Si/Si_{1-x}Ge_x/Si$ HBT's are fabricated in a non-UHV epitaxial technology for the first time, and their electrical characteristics are modeled analytically.

The formation of parasitic potential barriers for electrons in the base of HBT's resulting from base dopant outdiffusion or non-abrupt interfaces is studied, together with the concurrent degradation of the electrical performance of the devices. This deleterious effect is especially severe in devices with narrow, heavily doped bases fabricated in an integrated circuit (IC) process because of the thermal budget employed. To alleviate this problem, intrinsic $Si_{1-x}Ge_x$ spacer layers can be inserted on both sides of the base to greatly improve device performance.

The tradeoff between the common-emitter current gain β and the Early voltage V_A (output resistance) in heterojunction bipolar transistors is investigated for the

first time. This tradeoff is important for analog applications of HBT's, and it is shown that thin, narrow-gap layers in the base close to the base-collector junction reduce the Early effect dramatically leading to a high Early voltage. It is further demonstrated that even small amounts of dopant outdiffusion from the $Si_{1-x}Ge_x$ base into the silicon collector degrade the Early voltage drastically.

Finally, a novel Double-Base HBT is developed which increases the functionality of a HBT. Temperature-dependent measurements prove that the DC characteristics of the DB-HBT can be modeled using a version of charge-control theory. Switching is demonstrated in a single-transistor NAND gate at temperatures up to 150 K.

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Introduction

1.1 Current Trends and Limitations of VLSI

Despite much research on alternative technologies, silicon integrated circuits still dominate mainstream electronics. Scaling the feature sizes of the individual transistors and increasing the die size both allow one to increase the number of devices per chip. This reduces the chip count in electronic systems by providing more functionality per chip which results in lower system cost and increased reliability. The two most important devices used in silicon technology, field effect transistors and bipolar (potential effect) transistors, each have their strengths and weaknesses. For digital circuit applications CMOS technology (complimentary metal oxide semiconductor) currently dominates because of its low power dissipation and high density of integration. CMOS is the technology of choice for microprocessors and dynamic random access memories (DRAM's). Bipolar transistors with their high transconductance have predominantly been used in analog applications such as small signal amplification and in high-speed digital circuits like emitter-coupled logic (ECL) used in mainframes. The main drawback in bipolar digital circuits is the high power consumption requiring elaborate cooling systems and limiting integration. In an effort to improve single-chip functionality it is not surprising that despite increased process complexity BiCMOS processes have been developed to combine the advantages of CMOS and bipolar devices [1].

Examples of products already employing BiCMOS processes are high performance microprocessors and fast cache memories (SRAM's).

In this thesis exploratory silicon-based bipolar devices are investigated. In state-of-the-art, "conventional" bipolar technology, great emphasis is placed on decreasing the lateral and vertical dimensions of the individual transistors to both increase the speed of the "intrinsic" device and reduce parasitic capacitances and resistances due to the "extrinsic" device structure [2]. The most advanced conventional bipolar devices are fabricated in double-polysilicon, self-aligned processes using deep trench isolation [3]. Narrow bases are achieved by ion implantation. This thesis focuses on the vertical device profile of bipolar transistors and its implications for device performance. Two major deviations from standard silicon bipolar technology are employed: first, an epitaxial technique with improved control of the doping profile; Rapid Thermal Chemical Vapor Deposition (RTCVD) is used instead of ion implantation; and second, the heterojunction between the strained silicon-germanium ($Si_{1-x}Ge_x$) alloy and silicon is employed to control the shape of the potential barrier which the electrons see on their way from the emitter to the collector. The resulting $Si/Si_{1-x}Ge_x/Si$ heterojunction bipolar transistor (HBT) has improved performance compared to a homojunction device; process complexity, however, is increased.

1.2 Heterostructures for Electron Devices

Most of the electron devices employing heterojunctions have first been demonstrated in III/V materials systems such as AlGaAs/GaAs or InGaAs/InP which are lattice-matched, and for which epitaxial techniques have been developed to produce high quality interfaces at the heterojunctions such as Liquid Phase Epitaxy (LPE), Molecular Beam Epitaxy (MBE), or Metal-Organic Chemical Vapor Deposition (MOCVD). Varying the bandgap of the semiconductor enables the device designer to indepen-

dently control the forces acting on electrons and holes in the vertical device profile (the "central design principle" introduced by Kroemer [4]).

In the effort to further advance the limits of silicon technology it seems now feasible to incorporate epitaxially grown materials which form a heterojunction with silicon to improve device performance over homojunction devices. III/V layers crystallizing in the zincblende structure have been grown epitaxially on silicon, such as GaP on Si (which is lattice-matched) or GaAs on Si, but in these polar/non-polar heterostructures the formation of antiphase domains and cross-doping at the heterojunctions degrade their electronic properties [5, 6, 7]

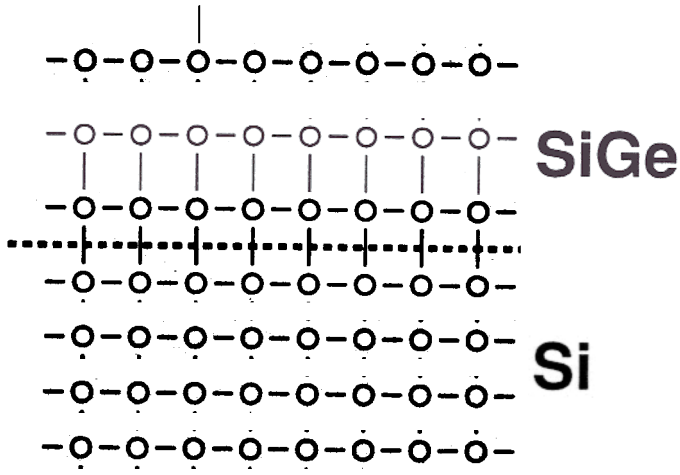
Cross-doping can be avoided in heterostructures formed by a column-IV element (C, Si, Ge, Sn), compound (e.g. SiC), or random alloy ($C_xSi_yGe_{1-x-y}$), and a silicon substrate. In these heterostructures the epitaxially grown film is usually not lattice-matched to silicon resulting in either strained layer growth or the formation of misfit dislocations at the heterointerface. Stoichiometric cubic β-silicon carbide (β-SiC) which has a lattice mismatch of 20% compared to silicon and a room temperature bandgap of 2.35 eV has been grown epitaxially on silicon by various methods. In chemical vapor deposited films, growth temperatures of over 1000°C were typically required to obtain single-crystalline films from multiple precursors (e.g. $SiHCl_3$, C_3H_8, and H_2) [8] which prevented their use in device structures containing thin, highly doped layers because of dopant diffusion [9, 10]. Using a single precursor, methylsilane ($SiCH_3H_3$), β-SiC films were grown at a temperature of only 750°C, but no electron devices have been demonstrated in these films so far [11]. Another recent effort focused on pseudomorphic, strained Si_xC_{1-x} and $C_xSi_yGe_{1-x-y}$ alloys, which could be grown with C concentrations up to a few % by MBE despite the small C solubility in Si of 10^{-4} at. % [12].

The $Si_{1-x}Ge_x$/Silicon Heterostructure

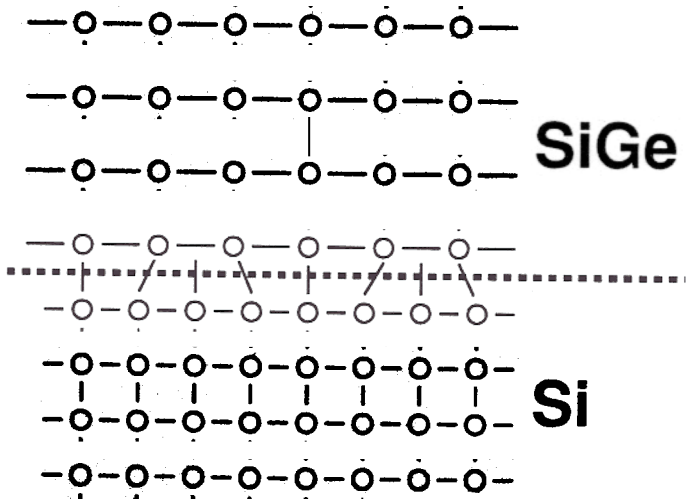
The epitaxial growth of the random $Si_{1-x}Ge_x$ alloy on <100> Si substrates has been the focus of intense investigation in the last decade. The methods used to grow high quality $Si_{1-x}Ge_x$ epitaxial films include molecular beam epitaxy (MBE) [13, 14], chemical vapor deposition (CVD) [15], ultra-high vacuum chemical vapor deposition (UHV-CVD) [16, 17], limited reaction processing (LRP) [18, 19], rapid thermal chemical vapor deposition (RTCVD) [20], and atmospheric-pressure chemical vapor deposition (APCVD) [21].

Since Ge and Si have a lattice mismatch of about 4%, the lattice constant perpendicular to the growth direction of the $Si_{1-x}Ge_x$ alloy can vary between the value of silicon and the value of the unstrained, cubic $Si_{1-x}Ge_x$ alloy obtained by interpolation between Si and Ge (Vegard's law). If the $Si_{1-x}Ge_x$ alloy grows without misfit dislocations on the silicon substrate (pseudomorphic growth), shown in Fig. 1.1 (a), the cubic lattice of the alloy is tetragonally distorted resulting in strain energy stored film.

If strained $Si_{1-x}Ge_x$ epitaxial layers are grown thicker than a certain *critical thickness* which depends on Ge concentration, it is energetically favorable for them to release strain by incorporating misfit dislocations at the heterointerface, as shown schematically in Fig.1.1 (b). These defects can be electrically active resulting in increased leakage currents in reverse-biased or in increased recombination currents in forward-biased *p-n* junctions [22]. Various theories to calculate the critical thickness have been developed, which usually assume that the heterostructure is in thermal equilibrium, i.e. in the state of its lowest total energy [23, 24, 25, 26, 27] (see Fig. 1.2). They do not take into account that there can be kinetic limitations preventing a pseudomorphically grown structure with a thickness above the critical thickness from relaxing towards its equilibrium state. $Si_{1-x}Ge_x$ layers in this metastable state



strained SiGe
⇒ few misfit dislocations at $Si/Si_{1-x}Ge_x$ interface



relaxed SiGe
⇒ many misfit dislocations at $Si/Si_{1-x}Ge_x$ interface

Figure 1.1: Schematic comparison between (a) strained (pseudomorphic) and (b) relaxed layer growth.

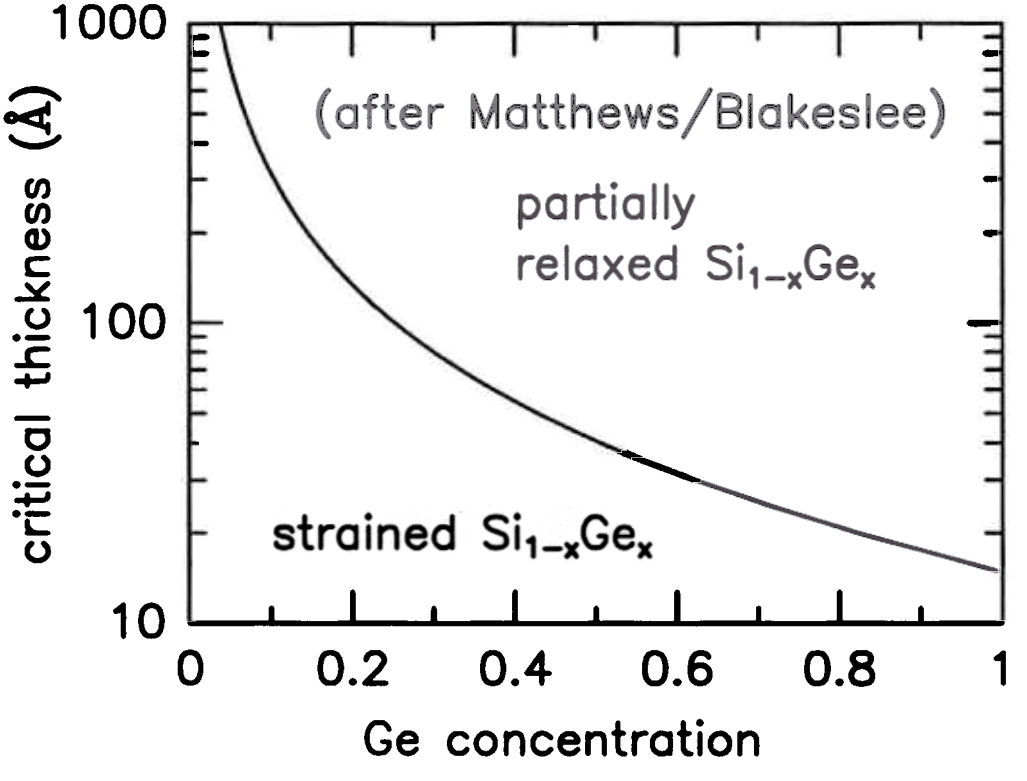


Figure 1.2: Equilibrium critical thickness of a pseudomorphic $Si_{1-x}Ge_x$ alloy epitaxial layer on a <100> silicon substrate after Matthews and Blakeslee.

will return to their equilibrium state if subjected to high temperatures; if they are incorporated into electron devices which are sensitive to misfit dislocations, high temperature processing steps should be minimized, resulting in a "low thermal budget" process.

The strain in an epitaxially grown $Si_{1-x}Ge_x$ alloy layer has important consequences for the electronic band structure. We focus here on the properties of strained $Si_{1-x}Ge_x$ layers on a <100> silicon substrate, since they are the most relevant for $Si/Si_{1-x}Ge_x/Si$ heterojunction bipolar transistors, the topic of this thesis. In an unstrained $Si_{1-x}Ge_x$ alloy, the conduction band minima are silicon-like (i.e. six degenerate valleys in the {100} directions) up to Ge concentrations of about 80%, and the bandgap reduction compared to silicon is fairly small as shown in Fig. 1.3 [28]. The strain in the alloy removes the six-fold degeneracy in the conduction band as well as the two-fold degeneracy between light and heavy hole in the valence band, resulting in a stronger bandgap reduction in the strained $Si_{1-x}Ge_x$ alloy [29, 30, 31], also shown in Fig. 1.3. Bandgaps corresponding to the wavelengths of 1.3 μm and 1.5 μm which are important for fiber-optic communication are obtained with moderate Ge concentrations. Fig. 1.4 shows the band lineup of conduction and valence band at the $Si_{1-x}Ge_x/Si$ heterojunction, a key parameter for device applications. For moderate Ge concentrations in the alloy a Type-I band lineup has been calculated [30, 32] and observed experimentally [33]. Most of the bandgap difference ΔE_G occurs as a valence band discontinuity ΔE_V, and the conduction band discontinuity ΔE_C is small.

Device Applications of $Si_{1-x}Ge_x$ Epitaxial Layers

Using pseudomorphic, strained $Si_{1-x}Ge_x$ epitaxial layers on silicon or $Si_{1-y}Ge_y$ buffer substrates, many devices previously restricted to III/V materials systems have been

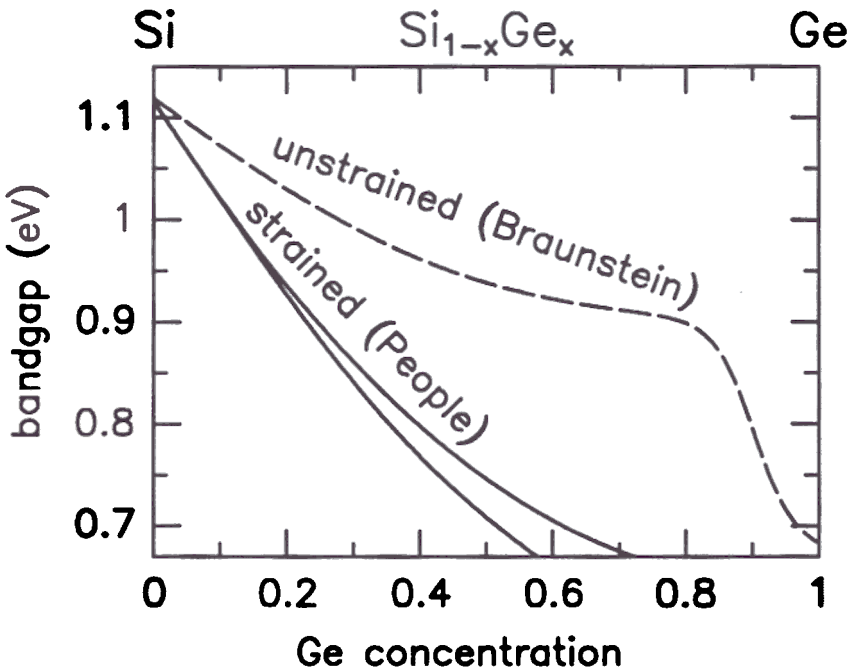
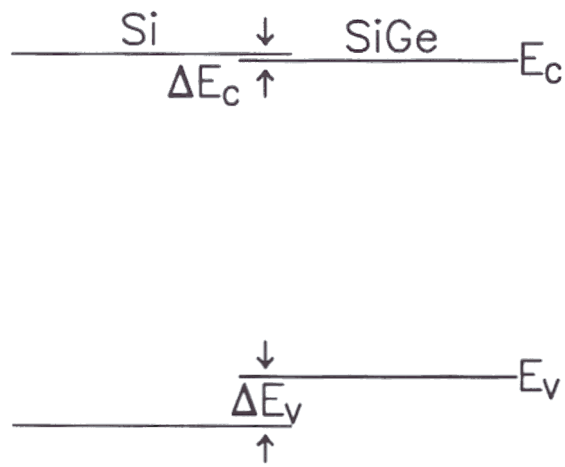


Figure 1.3: Bandgap of the strained and unstrained random $Si_{1-x}Ge_x$ alloy vs. Ge concentration, after People *et al.* and Braunstein *et al.* respectively.



$$Si_{0.80}Ge_{0.20}: \ \Delta E_C \approx 20 \text{ meV}, \ \Delta E_V \approx 148 \text{ meV}$$

Figure 1.4: Band lineup of a strained $Si_{1-x}Ge_x$ layer grown on a <100> Si substrate for germanium concentrations of less than about 60%.

demonstrated, including infrared waveguide photodetectors [34, 35, 36], resonant tunneling diodes [37, 38], modulation-doped field effect transistors (MODFET's) [39, 40], and bipolar inversion-channel field-effect transistors (BICFET's) [41, 42, 43].

More recently, devices utilizing the unique properties of the $Si/Si_{1-x}Ge_x$ materials system (heterojunction, high quality oxide) have been demonstrated, e.g. MOS-high hole mobility transistors (MOS-HHMT's) in which strained $Si_{1-x}Ge_x$ layers were incorporated into *p*-MOSFET's to increase their transconductance [44, 45, 46]. In these devices, the holes travel in a $Si_{1-x}Ge_x$ channel close to the oxide gate where they have a higher mobility than at the Si/SiO_2 interface. Various optical detectors based on internal photo-emission [47], and room temperature operation of 1.3 μm and 1.5 μm $Si/Si_{1-x}Ge_x$ quantum well LED's [48] promise to incorporate optical functions into standard integrated circuit technology.

Heterojunction Bipolar Transistors

Since the development of growth techniques for high-quality heterostructures much activity has been focused on heterojunction bipolar transistors (HBT's). The idea of varying the bandgap in a bipolar transistor structure to increase emitter injection efficiency dates back to Shockley who obtained a patent [49]. It expired before the first working devices were published [4], because bipolar devices require material with a high minority carrier lifetime and heterostructures with a defect-free interface, which could not be obtained before sophisticated growth techniques like liquid phase epitaxy (LPE), CVD, or MBE were developed.

Fig. 1.5 shows the band diagram (conduction and valence band vs. vertical distance) of a *npn*-bipolar transistor. In forward-active mode, the base-emitter junction is forward-biased by the input voltage (base-emitter voltage) V_{BE}, and the base-collector junction is reverse-biased by the output voltage (base-collector voltage) V_{CB}.

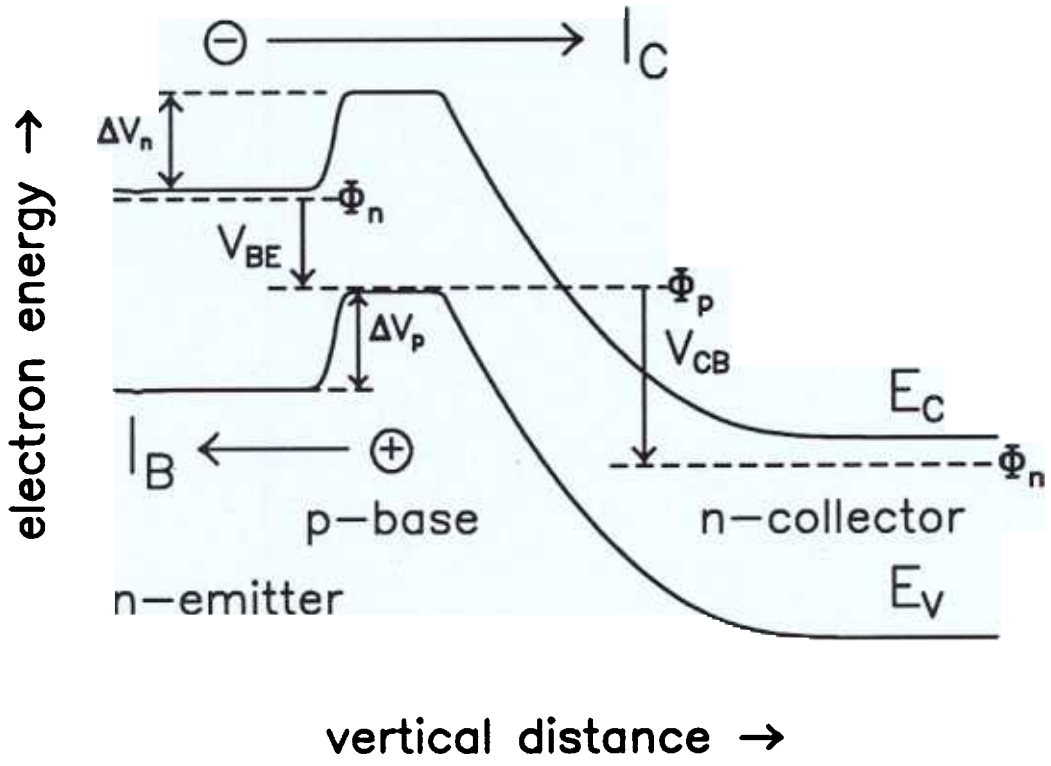


Figure 1.5: Simulated band diagram of a *npn*-bipolar transistor (emitter doping $N_D = 5 \times 10^{19}$ cm^{-3}, base doping $N_A = 2 \times 10^{18}$ cm^{-3}, base width $W_B = 500$ Å). In forward-active mode, the base-emitter junction is forward-biased (V_{BE}) and the base-collector junction is reverse-biased (V_{CB}). Electrons traveling from the emitter through the base into the collector constitute the output (collector) current I_C, while holes injected from the base into the emitter are the dominant component of the input (base) current I_B.

The *output current* (collector current I_C) consists of electrons which are injected from the n-emitter into the thin p-base, move through the base by drift and diffusion, and are collected in the n-collector layer (a drift field in the base can be caused by either a doping or a bandgap gradient, see Chapter 4). The number of electrons injected into the emitter side of the base is determined by the height of the potential barrier ΔV_n in the *conduction* band between the emitter and the base, which can be controlled by the input voltage V_{BE}. The dominant component of the *input current* (base current I_B) consists of holes which are injected from the p-base into the n-emitter (no holes are injected into the n-collector in forward active mode, because the base-collector junction is reverse-biased). The number of holes injected into the emitter is determined by the potential barrier ΔV_p in the *valence* band between base and emitter, which is also controlled by the input voltage V_{BE}.

The key idea of a heterojunction bipolar transistor is to lower the potential barrier seen by the carriers responsible for the *output* current (electrons in *npn* devices) compared with the one seen by the carriers constituting the *input* current (holes in *npn* devices), thereby increasing the ratio of output to input current, the common-emitter current gain $\beta = I_C/I_B$ of the HBT [4]. This is done by fabricating the emitter and the base from materials with different bandgaps. Depending on the layer in which the bandgap is changed compared to a homojunction device, two HBT configurations can be distinguished: In a *narrow-bandgap base* HBT the bandgap in the base is lowered thereby increasing the collector (output) current (see Fig. 1.6), whereas in a *wide-bandgap emitter* HBT the bandgap in the emitter is increased compared to a homojunction device resulting in a lower base (input) current (see Fig. 1.7). In both cases the common-emitter current gain $\beta = I_C/I_B$ is increased by a factor proportional to $\exp(\Delta E_G/k_BT)$ if spike-and-notch effects at the heterojunctions are neglected. Note that in HBT's where the emitter bandgap is larger than that in the base the current gain β should *increase* when the temperature is lowered, making it

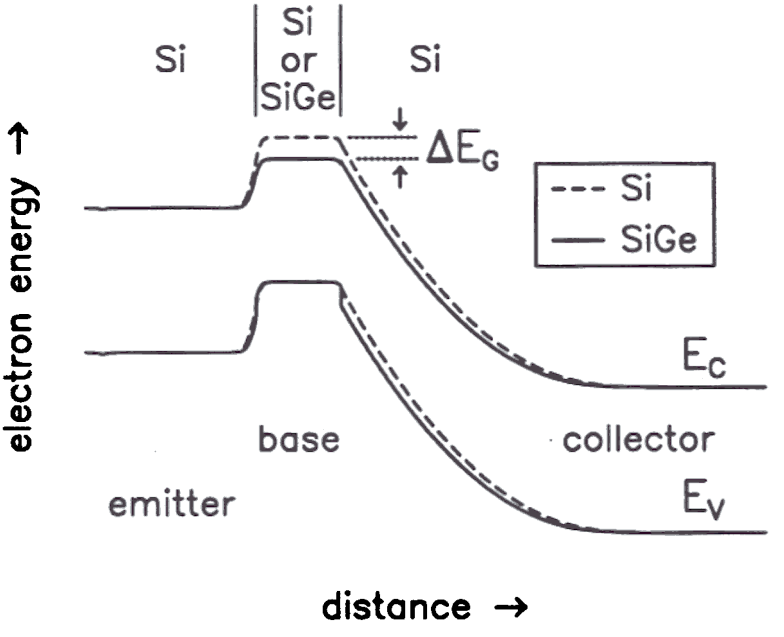


Figure 1.6: Band diagram of narrow-bandgap base *npn*-HBT. Lowering the conduction band barrier for electrons between the emitter and collector layers by decreasing the base bandgap increases the output (collector) current I_C and the common-emitter current gain $\beta = I_C/I_B$.

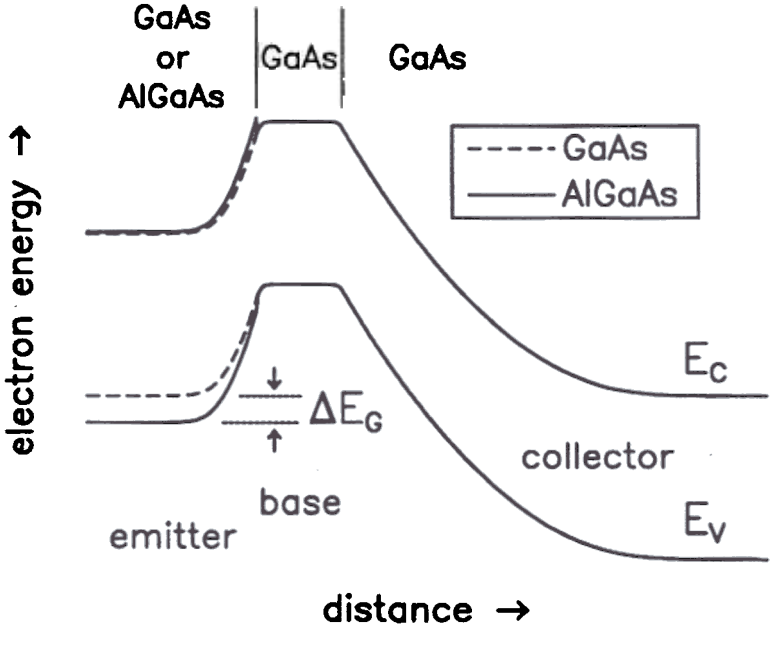


Figure 1.7: Band diagram of wide-bandgap emitter *npn*-HBT (emitter doping $\ll$ base doping). Increasing the valence band barrier for holes injected into the emitter lowers the input (base) current I_B increasing the common-emitter current gain $\beta = I_C/I_B$.

possible to operate the transistors at cryogenic temperatures. Since $Si/Si_{1-x}Ge_x/Si$ HBT's are the topic of this thesis, a more detailed description of their electrical characteristics will be presented in Chap. 3.

The first working heterojunction bipolar transistors were demonstrated in the III/V materials systems (for a review, see Ref. [4]). Since the (vertical) distance the carriers move from emitter to collector can be controlled very accurately and made very small using epitaxial techniques (100–1000 Å), HBT's are inherently fast devices if the parasitic capacitances and resistances related to the device structure are minimized; cutoff frequencies f_T in excess of 100 GHz were demonstrated in InGaAs/InP HBT's [50] and maximum oscillation frequencies f_{max} of 350 GHz were achieved in AlGaAs/GaAs HBT's [51].

Conceptually the simplest way to incorporate a heterojunction into a silicon bipolar transistor process is to replace the poly-silicon emitter of a standard bipolar process featuring self-alignment and deep trench isolation (e.g. Ref. [3]) with a wide-bandgap material having a high-quality interface to the silicon base, thereby combining the minimized parasitic capacitances and resistances of the device structure with the increased emitter injection efficiency of the wide-bandgap emitter HBT. Several wide-bandgap materials have been investigated, such as GaP [5, 6, 7], semi-insulating polycrystalline silicon (SIPOS) [52, 53, 54], oxygen-doped silicon epitaxial films (OXSEF) [55], epitaxial β-SiC [9], polycrystalline β-SiC [10], amorphous silicon (α-Si), and microcrystalline (μc-Si) silicon [56, 57, 58]. Major problems encountered were antiphase domains and cross-doping (GaP), high bulk or contact resistance (SIPOS, OXSEF, α-Si, poly-β-SiC), and high processing temperatures (single-crystalline β-SiC). As discussed above, β-SiC can now be grown at 750°C greatly improving its prospects for integration into Si HBT's with narrow, heavily doped bases. A key point in the wide-bandgap emitter on silicon HBT's is that the shape of the conduction band barrier in the base is identical to the one in a Si homojunction transistor. It is therefore

impossible to obtain the improvements of transit time and output resistance associated with a *bandgap grading* between the emitter and collector side of the base leading to a built-in drift field for the minority carriers in the base (see Chapters 3 and 6). A graded bandgap in the base is especially beneficial to overcome the retrograde drift field introduced by a doping profile which increases with depth, as is the case in devices using a $n^+/n^-/p^+/\ldots$ emitter-base structure with a lightly doped silicon emitter spacer to reduce tunneling current and base-emitter capacitance (see Section 5.3).

1.6 $Si/Si_{1-x}Ge_x/Si$ Heterojunction Bipolar Transistors

Despite the increased process complexity, much research has been done recently on silicon-based HBT's with bases consisting of the strained, narrow-bandgap $Si_{1-x}Ge_x$ random alloy. The first $Si/Si_{1-x}Ge_x/Si$ HBT's were fabricated from layers grown by MBE [59, 60, 61, 62, 63, 64, 65] (for a review see Ref. [66]). The base (input) currents in these devices were generally non-ideal because of defects at the $Si/Si_{1-x}Ge_x$ heterojunctions, low minority carrier lifetime in the $Si_{1-x}Ge_x$ layer, or deficiencies in the device structure. Then King *et al.* demonstrated the first $Si/Si_{1-x}Ge_x/Si$ HBT's with layers grown by a non-UHV CVD technique (limited reaction processing), employing junction-isolated, planar base-emitter junctions. In these devices the current gains were constant over several decades of output current despite the fact that the $Si_{1-x}Ge_x$ base layers were contaminated with high levels of oxygen [67, 68, 22], and it was also demonstrated that the onset of strain relaxation by incorporation of misfit dislocations is reflected in increased, nonideal base currents. The base current of a $Si/Si_{1-x}Ge_x/Si$ HBT is a very sensitive probe for the minority carrier lifetime in the base. Near-ideal base currents in the HBT's dominated by hole-injection into the emitter were achieved in devices fabricated by UHV-CVD, RTCVD, and MBE

[69, 70, 71, 72], proving that high lifetime material can be grown with any of these techniques. In the devices described so far the whole layer sequence was grown *in situ*, and the devices were not optimized for high-frequency operation. Process integration issues of $Si_{1-x}Ge_x$ layers have been studied in detail at IBM, and graded base $Si/Si_{1-x}Ge_x/Si$ HBT's were incorporated into a standard poly-emitter bipolar process with $Si_{1-x}Ge_x$ layers grown by UHV-CVD at 550°C [69]. Devices were then optimized for high-speed operation showing the leverage of the $Si/Si_{1-x}Ge_x$ heterojunction in standard Si technology, with cutoff frequencies of 75 GHz in the $Si_{1-x}Ge_x$ devices [73, 74], and ring-oscillators with ECL gate delays below 30 ps were demonstrated [75], with a relatively small improvement of only about 1 ps compared to all-silicon devices, however. Despite the leverage of a heterojunction in silicon bipolar technology the cost-effectiveness of this approach remains in doubt, since aggressive scaling of standard silicon homojunction transistors can provide similar circuit improvements in digital circuits [76]. More research is also needed to determine whether the low-temperature epitaxial technologies used for the $Si_{1-x}Ge_x$ layer growth can yield the low defect counts necessary for VLSI-type applications.

Contributions of this Thesis to the State-of-the-Art

In this thesis the improved control by RTCVD of the vertical profile of a $Si/Si_{1-x}Ge_x/Si$ HBT is used to study the effect of the shape of the potential barrier in the base seen by electrons on their way from the emitter to the collector on device performance:

- Near-ideal base currents in $Si/Si_{1-x}Ge_x/Si$ HBT's are achieved using a non-UHV technique for the first time, proving that high-lifetime $Si_{1-x}Ge_x$ material can be fabricated using processes compatible with standard silicon technology, i.e. chemical vapor deposition at reduced pressure (LP-CVD).

- Graded-base Si/$Si_{1-x}Ge_x$/Si HBT's are fabricated in a non-UHV epitaxial technology for the first time, and their electrical characteristics are modeled analytically using charge-control theory.

- The formation of parasitic potential barriers for electrons in the base of HBT's resulting from base dopant outdiffusion or non-abrupt interfaces is studied, together with the concurrent degradation of the electrical performance of the devices. This deleterious effect is especially important in devices with narrow, heavily doped bases fabricated in an IC process because of the thermal budget employed. It is then shown that intrinsic $Si_{1-x}Ge_x$ spacer layers inserted on both sides of the base alleviate this problem and allow one to increase the thermal budget of the process.

- The tradeoff between the common-emitter current gain β and the Early voltage V_A (a figure of merit proportional to the output resistance) in heterojunction bipolar transistors is investigated for the first time. This tradeoff is important for analog applications of HBT's, and it is shown that thin, narrow-bandgap layers in the base close to the base-collector junction reduce the Early effect drastically leading to a high Early voltage. It is also demonstrated that even small amounts of dopant outdiffusion from the $Si_{1-x}Ge_x$ base into the silicon collector severely degrade the Early voltage, and therefore have to be avoided in analog applications of Si/$Si_{1-x}Ge_x$/Si HBT's.

- A novel Double-Base HBT is developed which increases the functionality of an HBT. Temperature-dependent measurements prove that the DC characteristics of the DB-HBT can be modeled using an extension of charge-control theory. Switching is demonstrated in a single-transistor NAND gate at temperatures up to 150 K.

Chapter 2

Introduction to $Si/Si_{1-x}Ge_x/Si$ HBT's

In this chapter we continue the description of heterojunction bipolar transistors from Chap. 1.5, focussing on narrow-bandgap base $Si/Si_{1-x}Ge_x/Si$ HBT's. First, we discuss some figures of merit for individual devices. Then we describe briefly how the improvements possible in HBT's translate into faster digital circuits.

2.1 The Collector Current in $Si/Si_{1-x}Ge_x/Si$ HBT's

In a *npn* bipolar transistor the output (collector) current is controlled by applying a forward bias V_{BE} to the base-emitter junction. In forward active mode, the base-collector junction is reverse-biased by V_{CB}, as shown in the band diagram of Fig. 2.1. Electrons are injected into the base because the potential barrier ΔV_n they see between emitter and base is lowered by V_{BE}. In the *p*-type base the electrons are minority carriers, and they move by drift and diffusion to the collector side of the base where they are swept into the collector by the reverse-biased base-collector junction (V_{CB}). For constant base doping and bandgap, the electrons see no accelerating electric field in the base and they move by diffusion only. If the base material has a high minority carrier lifetime, which is usually the case in silicon homojunction transistors, very few electrons are lost in the base due to recombination with holes. If the doping N_A, the electron diffusion coefficient D_n, and the intrinsic carrier concentration n_i

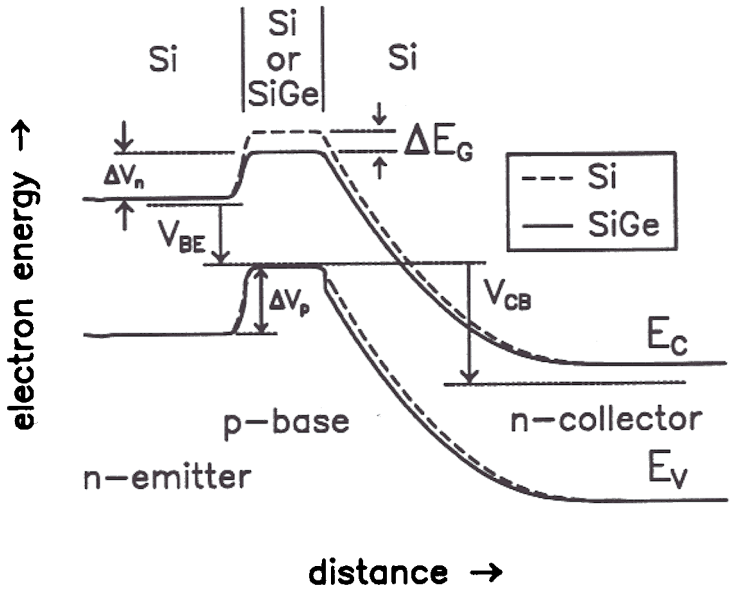


Figure 2.1: Band diagram of narrow-bandgap base HBT. In forward active mode, the base-emitter junction is forward-biased (V_{BE}) and the base-collector junction reverse-biased (V_{CB}).

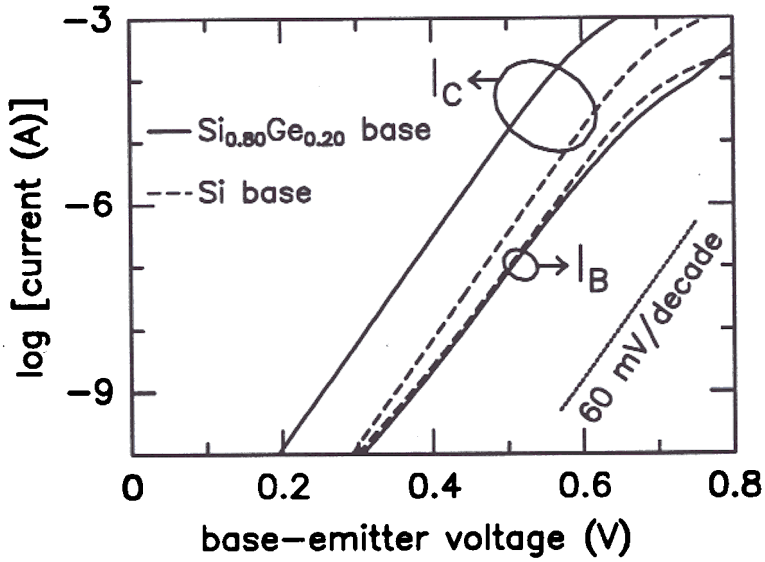


Figure 2.2: Room temperature Gummel plots (base and collector current vs. V_{BE} for zero base-collector bias) of flat base heterojunction bipolar transistor (solid lines) and silicon control device (dashed lines) with similar base sheet resistances, and emitter areas of 62×62 μm^2, showing the increased collector current due to the narrow-bandgap base.

are constant in the base, the collector current density is given by

$$J_C = qD_n \frac{\partial n}{\partial x} = qD_n \frac{n(BC) - n(BE)}{W_B} = -\frac{qD_n\, {n_{i,base}}^2}{N_A W_B}\, e^{qV_{BE}/k_BT}$$

where n is the electron concentration and W_B is the width of the neutral base [77]. $n(BE)$ and $n(BC)$ are the electron concentrations at the emitter and the collector side of the neutral base. Since the base-collector junction is reverse-biased, $n(BC) \approx 0$. The integrated doping concentration in the base, $N_A W_B$, is called the *Gummel number* N_G [78].

Fig. 2.1 shows the band diagram of a narrow-bandgap $Si_{1-x}Ge_x$ base heterojunction bipolar transistor with constant Ge concentration (and therefore bandgap) in the base ("flat base HBT"). Also shown is the band diagram of a silicon homojunction device for comparison. In the flat base HBT the potential barrier ΔV_n for electron injection into the base is lowered by the bandgap difference ΔE_G compared to the homojunction device, resulting in an exponential increase in collector current if there is no conduction band spike at the heterojunction:

$$\frac{J_C(SiGe)}{J_C(Si)} = \frac{\beta(SiGe)}{\beta(Si)} = \frac{D_n(SiGe)\, {n_{i,base}}^2(SiGe)\, N_G(Si)}{D_n(Si)\, {n_{i,base}}^2(Si)\, N_G(SiGe)} \propto e^{\Delta E_G/k_BT}$$

(first clearly demonstrated by King *et al.* [22]). This can also be seen in Eqn. 2.1, because the intrinsic carrier concentration in the base is exponentially dependent on the base bandgap, ${n_{i,base}}^2 \propto \exp(-E_G(base)/k_BT)$. Fig. 2.2 shows measured base and collector currents of a flat base $Si/Si_{0.80}Ge_{0.20}/Si$ HBT and a Si homojunction device, plotted logarithmically vs. base-emitter voltage at zero base-collector reverse bias. Both devices had similar pinched base sheet resistances of 2 kΩ/□ ($Si_{0.80}Ge_{0.20}$ base) and 3.6 kΩ/□ (Si base), indicating similar integrated base doping concentrations (Gummel numbers), and identical emitters and collectors. In this so-called *Gummel plot* the collector current of a bipolar transistor should be proportional to e^{qV_{BE}/k_BT} (see Eqn. 2.1) corresponding to an inverse slope of about 60 mV per decade

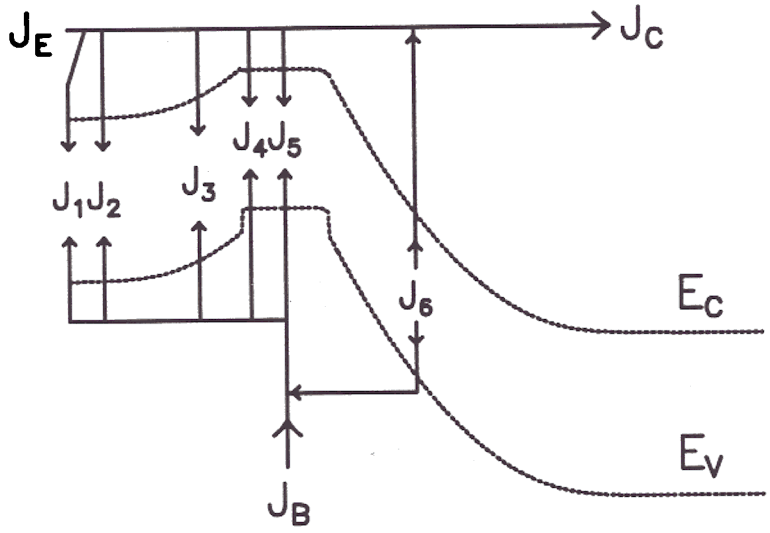


Figure 2.3: Sources of base current in narrow-bandgap base HBT. J_1 to J_5 are due to recombination at the emitter surface, in the neutral emitter, in the space-charge regions of the wide-bandgap emitter and the narrow-bandgap base, and the neutral base, respectively. Avalanche multiplication and thermal generation in the base-collector space-charge region (J_6) contribute to both base and collector current.

of collector current at room temperature. The $\approx 50\times$ increase in the collector current (and current gain) of the HBT compared to the homojunction transistor is due to the narrower bandgap in the base, since both devices had approximately the same integrated base dopant concentration.

2.2 The Base Current of Bipolar Transistors

The base (input) current of a bipolar transistor, which is desired to be much smaller than the collector (output) current, consists of several components as shown in Fig. 2.3. In the n-type emitter, holes can recombine with electrons at the emitter surface (J_1), in the neutral emitter (J_2), or in the wide-bandgap part of the base-emitter

space charge region (J_3). In the narrow-bandgap base, electrons can recombine with holes in the narrow-bandgap part of the base-emitter space charge region (J_4) or in the neutral base (J_5). An additional source of collector and base current consists of electron-hole pairs created by avalanche multiplication or thermal generation in the base-collector space charge region. The various base current components can be distinguished by their dependence on base-emitter voltage, base-collector voltage, and temperature. If both base and emitter material have a high minority carrier lifetime, which is usually the case in silicon homojunction transistors, the base current is dominated by J_1 or J_2. If the neutral emitter is wider than the hole diffusion length L_p, J_2 is given by:

$$J_2 = \frac{qD_p\, n_{i,emitter}^2}{N_D L_p}\, e^{qV_{BE}/k_BT} \qquad (2.3)$$

where N_D and L_p are emitter doping and hole diffusion length in the emitter, respectively. Eqn. 2.3 indicates that J_2 has an ideality factor η of one (η is defined by $J_2 \propto \exp(qV_{BE}/\eta k_BT)$). Fig. 2.1 shows that the potential barrier ΔV_p for hole injection into the emitter is the same for both the homo- and the narrow-bandgap heterojunction device, which implies that this component of the the base current should be identical in the two devices if they have similar emitters. This has indeed been observed in $Si/Si_{1-x}Ge_x/Si$ HBT's fabricated from layers grown by UHV-CVD, RTCVD, and MBE [69, 70, 71, 72], and is also evident from Fig. 2.2.

If the base current is dominated by neutral base recombination (J_5), and the base width W_B is much smaller than the electron diffusion length L_n in the base, the ideality factor η of the base current is still equal to one:

$$J_5 = \frac{q}{\tau_n}\int_{base} n(x)\, dx = \frac{qW_B\, n_{i,base}^2}{\tau_n}\, e^{qV_{BE}/k_BT}$$

where τ_n is the electron lifetime in the base. From Eqns. 2.1 and 2.4 the current gain $\beta = \tau_n/\tau_B$, where $\tau_B = W_B^2/2D_n$ is the base transit time for electrons. Hence, if the current gain is limited by neutral base recombination, it is a weak function of

temperature. This result allows one to obtain a lower limit for τ_n if β is known for a flat base homojunction or heterojunction transistor. The HBT of Fig. 2.2, e.g. had a current gain of about 100, a base width W_B of about 400 Å , and a base doping of 5×10^{18} cm^{-3}. If we assume that the electron diffusion coefficient D_n for $Si_{1-x}Ge_x$ is identical to the value in Si from Ref. [79] of 6.6 cm^2/Vsec we obtain a lower limit for τ_n of 120 ps. Note that in this device, however, the base current was limited by J_2, not by neutral base recombination, which we infer from the fact that the base currents of the HBT and the homojunction device were identical.

2.3 Figures of Merit of Bipolar Devices

For the characterization of bipolar devices several figures of merit have been developed. We have already introduced the common-emitter current gain $\beta = I_C/I_B$. Eqns. 2.1 and 2.3 show that if the base current is dominated by hole injection into the emitter (ideal case), β is proportional to $(N_D L_p/N_A W_B)$. In a homojunction transistor, therefore, the emitter is usually much more heavily doped than the base $(N_D/N_A \approx 100...1000)$; in silicon transistors emitter doping levels of about 10^{20} cm^{-3} are commonly used. The high doping in the emitter has the undesirable side effect that because of the formation of impurity bands the bandgap appears narrower, which reduces the current gain [80]. Base doping levels are typically from 10^{17} cm^{-3} to 10^{18} cm^{-3}. Increasing the base doping further would lead to a parasitic base current due to tunneling in the p^+/n^+ junction and would decrease the current gain [81]. Eqn. 2.2 and Fig. 2.2 show that the current gain in a HBT is increased by the exponential factor $\exp(\Delta E_G/k_B T)$, compared to a homojunction device with the same Gummel number.

It is usually observed that the current gain β decreases at high frequencies. The frequency where it drops to unity is called *cutoff frequency* f_T, and it is related to

the transit time of electrons from the emitter to the collector, τ_{EC} [82]:

$$\frac{1}{2\pi f_T} = \tau_{EC} = \tau_E + \tau_B + \tau_{CC} + \tau_C$$

where τ_{EC} is the sum of transit times through the emitter (τ_E), the base (τ_B), the base-collector depletion region (τ_{CC}), and the collector (τ_C). The base transit time τ_B can be greatly reduced by introducing a built-in drift field by either grading the base doping profile, or, in HBT's, grading the base bandgap, which will be discussed in Chap. 4. Since no high-frequency measurements will be presented in this thesis, we will not elaborate on the other delays any further.

The frequency at which the power gain reaches unity is called *maximum frequency of oscillation* f_{max}. It depends both on the intrinsic device profile, characterized by f_T, and on the parasitic base resistance R_B and base-collector capacitance C_{BC}:

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_B C_{BC}}}$$

The base-collector capacitance depends on the technology used to isolate different transistors from each other; in state-of-the-art processes, this is accomplished with deep trenches plasma-etched around the collector.

The parasitic base resistance R_B has two components, the *extrinsic base resistance* $R_{B,x}$ (from the base terminal to the active base) and the *intrinsic base resistance* $R_{B,i}$ (from the edge of the active base to any point inside the base). In state-of-the-art bipolar devices, the extrinsic base resistance is minimized by a base contact which is self-aligned to the emitter contact, i.e. both base and emitter contact are fabricated in *the same* photolithography step, and separated from each other by a distance smaller than the minimum photolithographic linewidth. The intrinsic base resistance is proportional to the *pinched base sheet resistance* $R_{B,sh}$, which depends on the base doping profile:

$$R_{B,sh} = \left(\int_{base} q\mu_p(x) N_A(x)\, dx \right)^{-1}$$

where μ_p is the in-plane hole mobility in the base, and the integral is taken over the neutral base. In a homojunction transistor, increasing the base doping to lower the base sheet resistance also lowers the current gain β, as can be seen from Eqn. 2.1, resulting in a tradeoff between β and $R_{B,sh}$. High-performance homojunction devices have an intrinsic base sheet resistance of more than 10 $k\Omega/\square$ [3].

A key advantage of the HBT is that the current gain improvement suggested by Eqn. 2.2 can be traded for a lower base sheet resistance by increasing the base doping to a value which can be higher than the emitter doping while still preserving sufficient current gain. In such a device, however, a lightly doped ($< 10^{18}$ cm^{-3}) silicon spacer layer between emitter and base has to be inserted to prevent a parasitic tunneling current between base and emitter, and to reduce base-emitter capacitance.

For analog applications of bipolar transistors, the product of β and the output resistance of the device is also important. It will be discussed in great detail in Chap. 6.

In digital circuit families like emitter-coupled logic (ECL), the figures of merit characterizing the device speed, f_T and f_{max}, have only a loose correspondence to the gate delay of the circuit. Expressions have been developed to characterize the gate delay as a function of device parameters and the operating point (current level) [83, 84]. At low current levels, the gate delay is dominated by the RC time constant of the load resistor and the parasitic device and load capacitances, while at high current levels, it is dominated by the RC time constant of the base resistance and the diffusion capacitance. The gate delay component corresponding to charge storage in the device, τ_{EC}, and the RC time constant of intrinsic base resistance and collector capacitance, are insensitive to the current level.

Since in ECL circuits a current gain of about 100 is usually sufficient, the key advantage of $Si/Si_{1-x}Ge_x/Si$ HBT's compared to homojunction devices is twofold: first, the intrinsic base sheet resistance can be lowered dramatically in a HBT while still

preserving sufficient current gain, because of the increased emitter injection efficiency of the $Si/Si_{1-x}Ge_x$ heterojunction; and second, using a graded bandgap base the base transit time can be reduced compared to a flat-base device. The latter approach has been taken by Burghartz *et al.* resulting in ECL circuits with gate delays below 30 ps in $Si/Si_{1-x}Ge_x/Si$ HBT's with a base grading of 0–11% Ge and a base sheet resistance of 8.3 kΩ/□ [75]. The fundamental problems related to the first approach, the integration of $Si/Si_{1-x}Ge_x/Si$ HBT's with low intrinsic base sheet resistance into an IC process, are addressed in Chap. 5.

Chapter 3

Growth and Processing of $Si/Si_{1-x}Ge_x/Si$ HBT's

In this chapter we first describe the growth of the epitaxial Si and $Si_{1-x}Ge_x$ layers by Rapid Thermal Vapor Deposition. Then the process developed for fabricating $Si/Si_{1-x}Ge_x/Si$ HBT's is outlined.

3.1 Growth of Silicon and $Si_{1-x}Ge_x$ Epitaxial Films by RTCVD

The silicon and $Si_{1-x}Ge_x$ epitaxial layers used in this work were grown in a homemade Rapid Thermal Chemical Vapor Deposition (RTCVD) reactor which features load-locked wafer exchange, external lamp heating, rapid gas switching, and a quartz stand instead of a susceptor.

The RTCVD reactor is schematically shown in Fig. 3.1 [20]. The growth chamber consists of a 17.5 cm diameter cylindrical quartz tube. On one end, the tube diameter is reduced, and the gas inlet connection is made using a compression O-ring fitting. The other end is attached to a stainless steel assembly using a flange with a double O-ring seal. The space between these O-rings is evacuated with a small rotary vane pump which prevents the contamination of the growth chamber if there are small leaks in the fitting. Attached to the stainless steel assembly are a rotary vane pump with a throttle valve for pressure control during epitaxy, and a load lock consisting of a loading chamber separated by a gate valve. The loading chamber can be evacuated

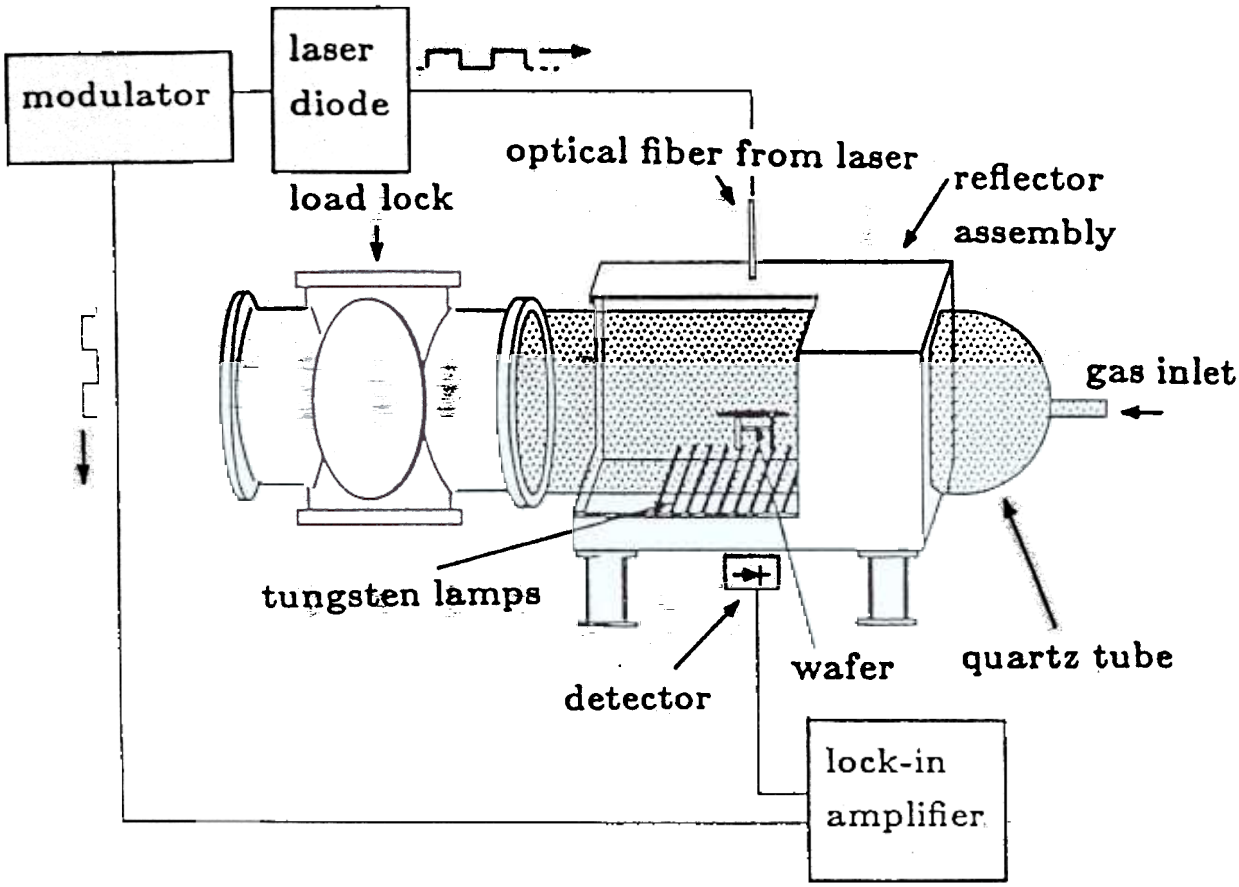


Figure 3.1: Schematic diagram of the Rapid Thermal Chemical Vapor Deposition reactor used in this work.

by a rotary vane pump, and special care is taken not to decrease the pressure in the loading chamber below the viscous flow regime which would result in pump oil backstreaming.

The gases used for growing $Si_{1-x}Ge_x$ layers are dichlorosilane ($SiCl_2H_2$), silane (SiH_4), and germane (0.8% GeH_4 in H_2). Doping is accomplished using diborane (10 ppm B_2H_6 in H_2) and phosphine (70 ppm PH_3 in H_2). These process gases are filtered for particles and for water vapor. They flow in hydrogen carrier gas which is purified by diffusion through palladium. The process gas mixture is established in a manifold containing mass flow controllers. Five-ported valves for rapid gas switching are used to inject the gases either into a vent line or into the growth chamber. During epitaxy, the gases are first injected into the vent line to establish the desired flow with the mass flow controller. Then they are injected into the hydrogen carrier gas entering the growth chamber.

During epitaxy, the wafer is heated by a bank of twelve 6 kW tungsten-halogen lamps for rapidly changing and optimizing the wafer temperature for each epitaxial layer. The wafer temperature has to be controlled accurately because the growth rate of silicon and $Si_{1-x}Ge_x$ alloy layers is a strong function of temperature.

The wafer temperature is measured accurately in the range between 600°C and 800°C using a method developed at Princeton [85]. Infrared light from two semiconductor lasers with wavelengths of 1.3 μm and 1.5 μm is transmitted through the quartz tube and the wafer and then detected using a photodiode. Before growth the room temperature transmission signal is measured. Since the intensity of the infrared light transmitted through the wafer at a temperature between 600°C and 800°C is a strong function of temperature, it can be used to measure temperature accurately. To compensate for reflections at the rough backside of the wafer, the transmitted signal is normalized by the room temperature transmission value. Since the backside polish of the wafer can change during epitaxy of thick layers resulting in an erroneous

temperature measurement, the room temperature transmission value is taken *after* the growth of the buffer layer.

At a pressure of 6 torr, silicon layers in the RTCVD reactor described above are grown at temperatures between 700°C (30 Å/min) and 1000°C (0.5 μm/min) using 26 sccm of dichlorosilane in 3 slpm of hydrogen. For $Si_{1-x}Ge_x$ alloy layers the temperature is lowered to 625–700°C depending on Ge concentration to suppress three-dimensional growth, and to allow the growth of metastable layers whose thickness exceeds the equilibrium critical thickness.

The epitaxial layers for this thesis were grown on 4-in diameter p-type or n-type <100> silicon wafers with a resistivity of 1–10 Ωcm. Before growing the epitaxial Si or $Si_{1-x}Ge_x$ layers, the wafers were cleaned in a hot 1:1 solution of H_2SO_4 and H_2O_2 which resulted in the growth of a thin chemical oxide. After a rinse in deionized water, the chemical oxide was removed in a 1:100 solution of hydrofluoric acid in water. The wafers were then blown dry in nitrogen and immediately loaded into the RTCVD reactor. This cleaning procedure resulted in a hydrogen-passivated, oxide-free surface [86].

For all transistor structures used in this thesis a high temperature cleaning step was performed before growing the epitaxial layers. It consisted of a 1 min bake in a hydrogen ambient at a temperature of 1000°C and a pressure of 250 torr which removed all remaining oxide from the silicon surface.

Then the pressure was lowered to 6 torr and a sequence of epitaxial layers was grown on a <100> silicon wafer as shown in Fig. 3.2. After growing the heavily doped n^+-silicon buffer layer the epitaxy was interrupted for 10 min to obtain the room temperature infrared transmission signal. Then the wafer was heated again to 1000°C for 1 min in hydrogen, followed by the growth of the collector layer at a temperature between 850°C and 1000°C.

In the first two runs (#121–123 and #246–261) the collector layers were grown at

Si	n-emitter	10^{17} cm^{-3}	3000 Å	850°C
$Si_{1-x}Ge_x$	p-base	10^{19} cm^{-3}	500 Å	625–800°C
Si	n-collector	10^{17} cm^{-3}	3000 Å	850–1000°C
Si	n^+-buffer	10^{19} cm^{-3}	1 μm	1000°C
<100> silicon substrate				

Figure 3.2: Typical layer sequence of $Si/Si_{1-x}Ge_x/Si$ heterojunction bipolar transistor structure.

850°C and doped with PH_3. Secondary Ion Mass Spectrometry (SIMS) on these layers showed phosphorus spikes at the $Si/Si_{1-x}Ge_x$ base-collector junction. They could have been caused by phosphorus segregation on the silicon surface during growth at 850°C and subsequent incorporation at the $Si/Si_{1-x}Ge_x$ interface upon lowering the temperature to 625°C. These spikes partially compensated the base. In the following run (#448–460) the collector was therefore grown at 1000°C. SIMS on these samples again showed phosphorus spikes (see Fig. 4.3).

In the final runs (#633–643, #932–949, and #1075–1078) the collector layers were again grown at 1000°C, but without doping the collector *in situ*. Phosphorus outdiffusion from the n^+ buffer into the undoped collector caused a doping profile which increased exponentially with depth.

The $Si_{1-x}Ge_x$ base layers with Germanium concentrations below 13% were grown at 700°C, and the layers with more than 13% Ge were grown at 625°C. In similar CVD systems which were not equipped with a load lock, these growth conditions resulted in high oxygen concentrations in the $Si_{1-x}Ge_x$ layers ($> 10^{20}$ cm^{-3}) [22]. Since the installation of our load lock, the oxygen concentration in the $Si_{1-x}Ge_x$ base layers was below the SIMS (Secondary Ion Mass Spectrometry) detection limit of about 10^{18} cm^{-3}. Finally the temperature was raised to 850°C to grow the lightly doped n-emitter.

A key issue for the performance of $Si/Si_{1-x}Ge_x/Si$ HBT's is the alignment of the base (boron) dopant interfaces (position of the p-n junctions) with the $Si/Si_{1-x}Ge_x$ interfaces, as will be discussed in Chap. 5. With RTCVD at temperatures below 700°C, this alignment can be controlled with an accuracy of < 10 Å, as has been demonstrated by Venkataraman *et al.* from measurements on normal and inverted modulation-doped two-dimensional hole gases [87].

3.2 HBT Process with Junction-Isolated Base and Emitter

The focus of this thesis has been on vertical carrier transport. The main goal of the HBT process developed for this work was therefore to obtain transistors with near-ideal base currents for DC measurements given the limited resources at Princeton. It was not attempted to scale the devices laterally, or to minimize parasitic resistances and capacitances.

The device structure was similar to the one described by King *et al.* [22], who also provided the mask set which was suitable for making three-terminal bipolar transistors in which the collector contact was made at the bottom of the wafer. For the process described here, the mask set was modified to obtain a collector contact on the top of the wafer. The transistor structure described here featured a junction-isolated base-emitter junction, a mesa-isolated base-collector junction, and a low thermal budget. Similar structures have been scaled down to achieve sub-μm emitter widths by Kamins *et al.*, but since the base contact is not self-aligned to the emitter contact it is difficult to obtain devices with low extrinsic base resistance [73].

The process flow is shown in Fig. 3.3. For contacting the base boron was implanted around the emitter using low-temperature (350°C) plasma-deposited silicon dioxide (p-SiO_2) as a mask, which is less dense than thermally grown SiO_2 and can contain hydrogen [88]. Its thickness was therefore chosen conservatively to be about twice the implant range for high-quality thermally grown SiO_2. Implant doses and energies were determined from SUPREM III simulations. Typically, a triple implant was used (1×10^{15} cm^{-2} BF_2^+, 40 keV; 2×10^{14} cm^{-2} B^+, 70 keV; 3×10^{14} cm^{-2} B^+, 100 keV). Since the implant surrounded the base-emitter junction, only a small part of the base-emitter depletion region around the contacts touched the silicon surface. This design minimized surface recombination, a parasitic component of the base current.

After the base implant, the plasma-deposited implanted oxide was removed and

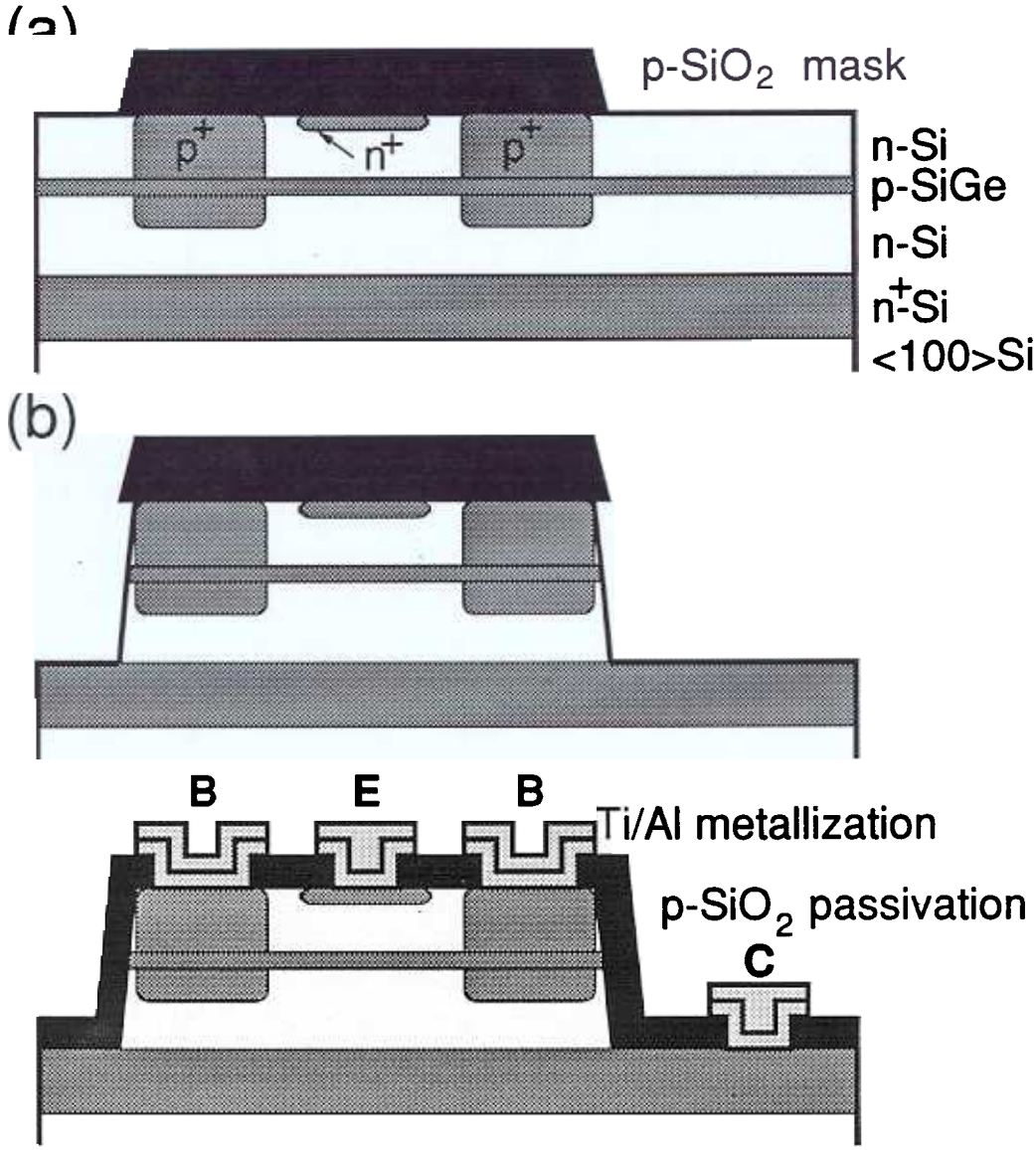


Figure 3.3: Process flow of junction-isolated bipolar transistor. The implant anneal was performed before the collector mesa etch.

new oxide deposited, followed by the emitter implant photolithography. Since the heavily implanted silicon was amorphous, it could be easily distinguished from crystalline silicon facilitating alignment of the emitter implant mask. After etching the implant windows using buffered oxide etch (1:6 HF in NH_4F), arsenic was implanted with a dose of 1×10^{15} cm^{-2} and an energy of 15 keV.

Since the plasma-etching system had been used before for etching silicon covered with gold contacts, the mesa was etched *after* the implant anneal to prevent the diffusion of gold into the transistor layers if contamination had occurred. After the implant anneal the implanted regions were no longer visible on the wafer. Therefore silicon dioxide was deposited first by plasma-deposition, and mesas were etched into the p-SiO_2 using the implants for alignment (see Fig. 3.3 (a)). Then the wafers were given a modified RCA clean (without the NH_4OH/H_2O_2 step, since it etched $Si_{1-x}Ge_x$ alloys), loaded into a furnace, and annealed at 700°C for 30 min in a nitrogen ambient resulting in sufficient activation of the implants. After the anneal, the base-collector junctions were isolated by etching mesas in a SF_6/CCl_2F_2 plasma down to the n^+ buffer layer (see Fig. 3.3 (b)).

Low temperature oxide was deposited for passivation, followed by contact hole photolithography and etch. After another modified RCA clean, the wafers were loaded into an e-beam evaporator for metallization Since aluminum alone diffuses rapidly in silicon and would spike to the base layer, a titanium layer (typically $>$ 1000 Å thick) acting as a diffusion barrier was inserted between the aluminum and the silicon. After etching aluminum (H_3PO_4 , HNO_3 , CH_3COOH , H_2O) and titanium (1:100 HF in H_2O), the wafers were annealed at 400°C in forming gas (10% H_2 in N_2) which resulted in improved base currents, since hydrogen passivated the dangling bonds at the silicon surface. The final device structure is shown in Fig. 3.3 (c). Note that an epitaxially grown heavily doped n^+ emitter layer would result in a n^+/p^+ junction where tunneling and subsequent recombination of electrons and holes would

cause a parasitic contribution to the base current [81].

The biggest devices measured had an emitter area of $62 \times 62\ \mu m^2$. All electrical measurements in this thesis were done on these devices, if not otherwise stated. The smallest working devices had an emitter area of $10 \times 10\ \mu m^2$.

Chapter 4

Graded Base $Si/Si_{1-x}Ge_x/Si$ HBT's

Introduction and Previous Work

Base transport of minority carriers in a HBT is determined by the position and the shape of the conduction band in the base. In devices with constant doping and bandgap profiles in the base, the conduction band position in a lightly doped homojunction transistor is equal to the one of a more heavily doped HBT, as shown in Fig. 4.1, making it possible to achieve similar current gain with lower base sheet resistance in the HBT. In bipolar transistors with constant base bandgap and doping profiles, the electrons see no aiding drift field in the base, and they move by diffusion

Soon after the bipolar transistor had been invented, however, Kroemer realized that a quasi-electric drift field seen by the minority carriers in the base can reduce the minority carrier transit time [89]. A quasi-electric field for electrons in the *p*-type base can be obtained by either grading the doping profile or the bandgap, as shown in Fig. 4.2. In state-of-the-art doubly ion-implanted homojunction transistors, graded doping profiles which decrease with depth are usually obtained, resulting in a drift field in the base. In HBT's, quasi-electric fields in the base can be created by grading the base bandgap from a wide gap at the emitter side of the base towards a narrow gap at the collector side.

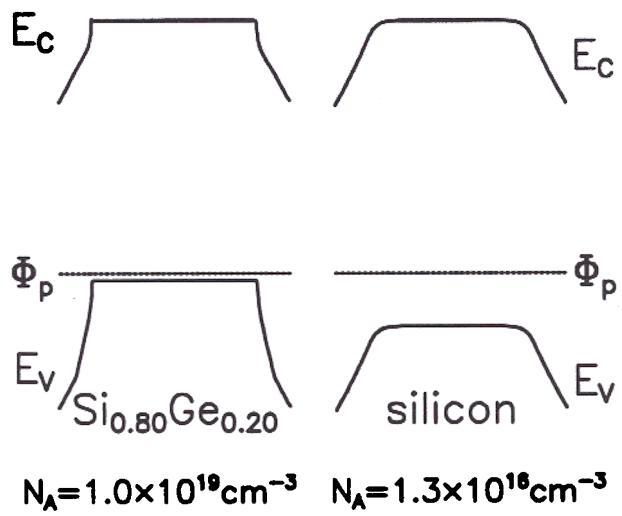


Figure 4.1: The position of the conduction band in the base with respect to the hole quasi-Fermi level Φ_p determines the collector current. The simulated band diagrams of the bases of a $Si/Si_{1-x}Ge_x/Si$ HBT and a silicon homojunction device show that reducing the bandgap in a narrow-gap base HBT has the same effect as reducing the doping in an all-silicon device.

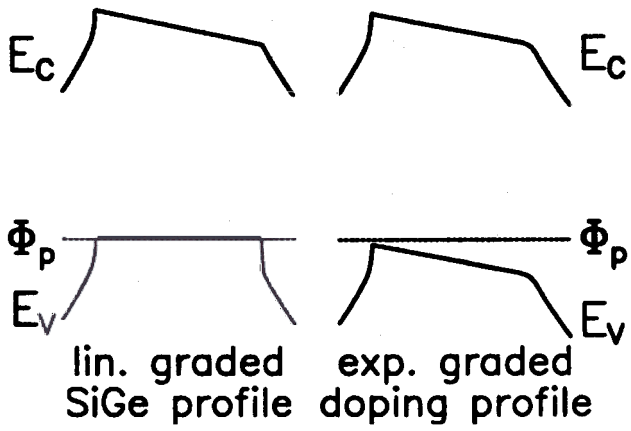


Figure 4.2: Simulated band diagrams of the bases of a $Si/Si_{1-x}Ge_x/Si$ HBT (left) and of a homojunction transistor (right), showing that constant quasi-electric fields seen by electrons in the base of a bipolar transistor can be obtained by either linearly grading the bandgap of a HBT or exponentially grading the base doping concentration of a homojunction device.

The effect of a graded bandgap base was demonstrated by Capasso *et al.* in a phototransistor [90], by Levine *et al.* who measured the electron velocity in a graded p^+-AlGaAs layer [91], and by Hayes *et al.* in an AlGaAs/GaAs HBT [92].

The first graded base $Si/Si_{1-x}Ge_x/Si$ HBT's were demonstrated by Narozny *et al.* [65]. In these devices, however, the Ge concentration in the base decreased from the emitter to the collector side introducing a retrograde drift field. At IBM, UHV-CVD was used to integrate a graded base HBT into a poly-emitter process [69], and near-ideal junction characteristics were obtained, with emitter-injection limited base currents which were independent of the Ge profile in the base.

In a $Si/Si_{1-x}Ge_x/Si$ HBT the base is already very thin resulting in a short base transit time. As shown in Chap. 2, however, heavy base doping implies that a n^- emitter spacer has to be used to prevent a p^+/n^+ tunnel junction, resulting in a *retrograde* doping profile at the emitter side of the base which increases base transit time. In such a device, a graded $Si_{1-x}Ge_x$ profile at the emitter side of the base can compensate for the retrograde field resulting in improved high frequency performance [74]. As will be shown in Chap. 6, grading the bandgap in the base also dramatically increases the output resistance (Early voltage).

In this chapter we demonstrate the first graded-base $Si/Si_{1-x}Ge_x/Si$ HBT's fabricated from layers grown with a non-UHV technique. Their near-ideal, emitter-injection limited base currents were independent of the base doping and Ge profiles [70, 93]. Current gains in excess of 11,000 at 133 K were observed. The temperature dependence of the collector currents is shown to obey a simple analytical model that can be applied to devices with arbitrary base profiles.

Table 4.1: Device structures of this experiment and measured values of β, V_A, and $R_{B,sh}$. Bandgap differences ΔE_G are from Ref. [30].

Device	633	450	449	448	458
%Ge at emitter side of base	0	0	7	13	20
$\Delta E_{G,1}$ (meV)	0	0	59	109	168
%Ge at collector side of base	0	20	20	20	20
$\Delta E_{G,2}$ (meV)	0	168	168	168	168
$R_{B,sh}$ (k$\Omega/\square$)	3.6	6.3	7.8	44.0	12.0
Ge base width (SIMS) (Å)	N/A	740	680	400	250
base doping (SIMS) ($\times 10^{18}$ cm^{-3})	N/A	2.3	2.3	1.1	5.5
forward β (293 K)	5	55	120	1300	1700
forward V_A (V)	100	86	35	5	10

Fabrication of Graded-Base $Si/Si_{1-x}Ge_x/Si$ HBT's

The vertical transistor structures discussed in this chapter are described in Table 4.1. All devices had identical emitter and collector layers. A control device had an all-silicon base, three graded base devices had germanium concentrations varying linearly from emitter to collector (0–20%; 7–20%; 13–20%), and a flat $Si_{1-x}Ge_x$ base HBT had a constant Ge concentration of 20%. The device structures were grown as described in Chap. 3.1. In the graded base devices, the nominally 500 Å thick bases were divided into ten 50 Å thick segments with constant Ge and doping concentrations (see Appendix B.2). The layers with more than 13% Ge were grown at 625°C and for less than 13% Ge the temperature was raised to 700°C to enhance the growth rate [94]. The flow of silane was kept constant at 26 sccm, while the GeH_4 flow was varied to adjust the Ge concentration in the layers. The diborane flow was also adjusted proportional to the assumed growth rate in each segment to achieve a constant base

doping of approximately 2–5 $\times$ 10^{18} cm^{-3}. All emitters were grown at 850°C and doped approximately 5 $\times$ 10^{17} cm^{-3} with a thickness of about 2500 Å. The device processing was identical to that described in Chap. 3.2.

A calibrated SIMS (Secondary Ion Mass Spectrometry) profile of structure #450 (0–20% Ge) is shown in Fig. 4.3. Note the fairly high collector doping of about 8 $\times$ 10^{17} cm^{-3} leading to a low breakdown voltage BV_{CEO} of about 2 V. In devices #448–460 the collector was grown at 1000°C and the growth was interrupted before growing the base at lower temperature to prevent the formation of a phosphorus spike at the base-collector junction which had been observed in earlier runs. Despite these precautions, however, a phosphorus spike was again clearly visible at the base-collector $Si/Si_{1-x}Ge_x$ interface, which could be due to residual phosphorus in the growth chamber and the increased sticking coefficient of phosphorus at low temperatures, or due to phosphorus segregation at the $Si/Si_{1-x}Ge_x$ interface [95]. It partly compensated the collector side of the base, an effect which was particularly severe in device #448 leading to a high base sheet resistance of 44 k$\Omega/\Box$ and an effective grading of only 13–15% Ge instead of the expected 13–20% Ge in this device. Note that the base dopings from Table 4.1 do not include the effect of the phosphorus spike. Fig. 4.4 shows the Ge profiles obtained by SIMS of the graded-base devices of Table 4.1, proving the control over the Ge profile possible with RTCVD, despite the fact that the temperature was changed while growing the $Si_{1-x}Ge_x$ base.

4.3 Electrical Measurements on Graded-Base Devices

Gummel plots of the five devices are shown in Fig. 4.5. Despite the different base doping and Ge profiles, the base currents were nearly identical with near-ideal slopes of about 60 mV/decade. Since all devices had the same emitter, the base current component originating from hole injection into the emitter should be the same in all

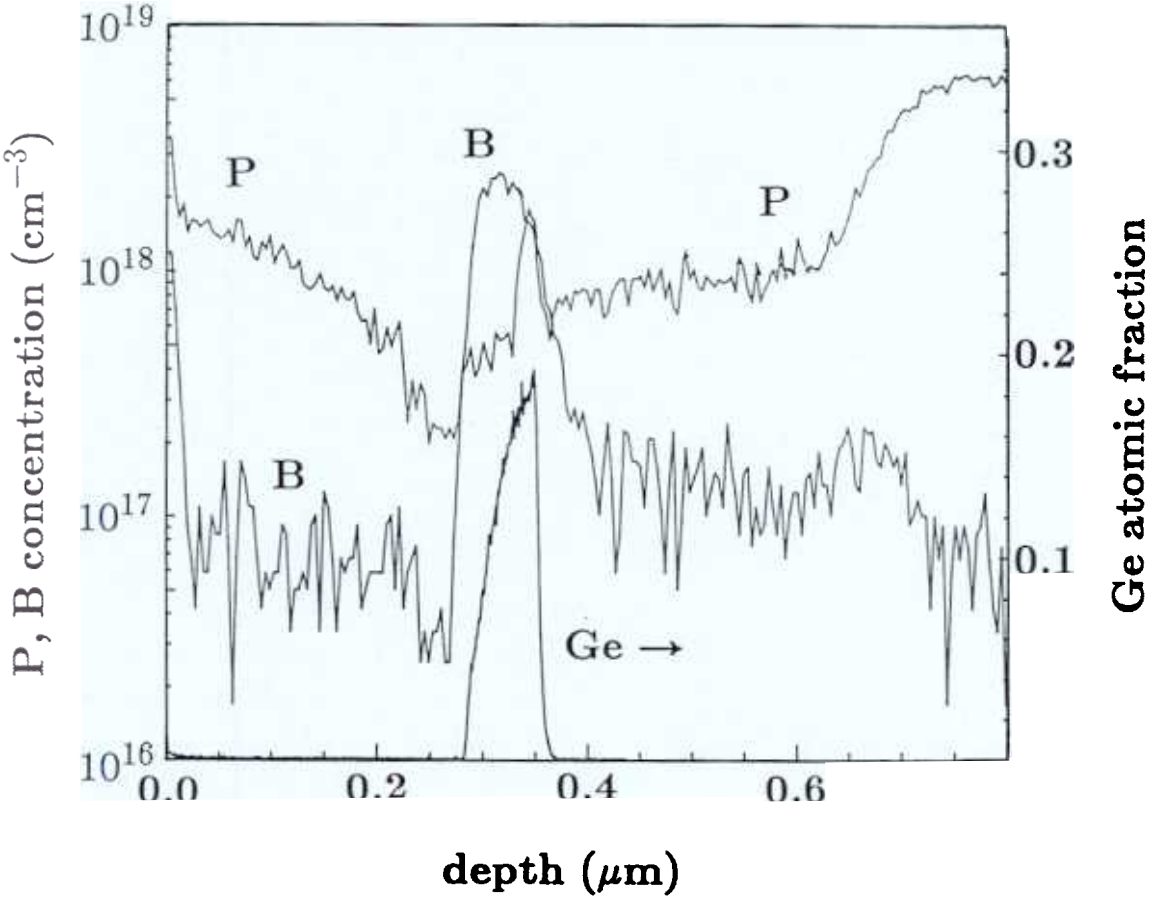


Figure 4.3: As-grown SIMS profile of device #450 (0–20% Ge) without the emitter implant. Note that the Ge profile is shown on a linear scale.

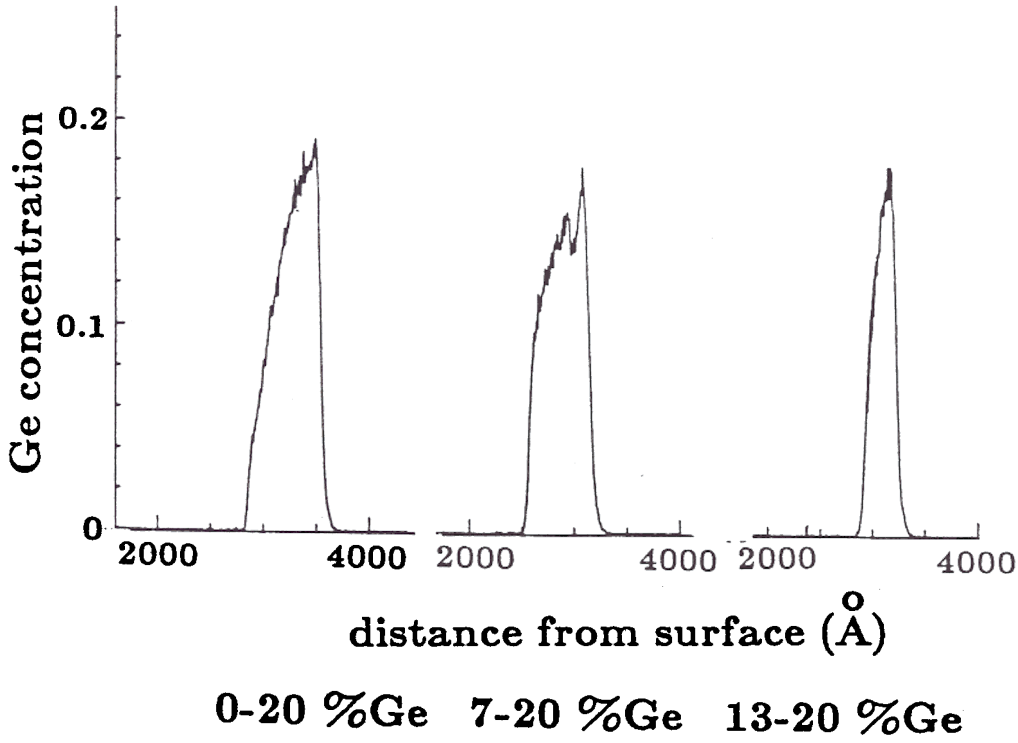


Figure 4.4: Ge profiles obtained by SIMS of the graded-base devices with 0–20% Ge, 7–20% Ge, and 13–20% Ge.

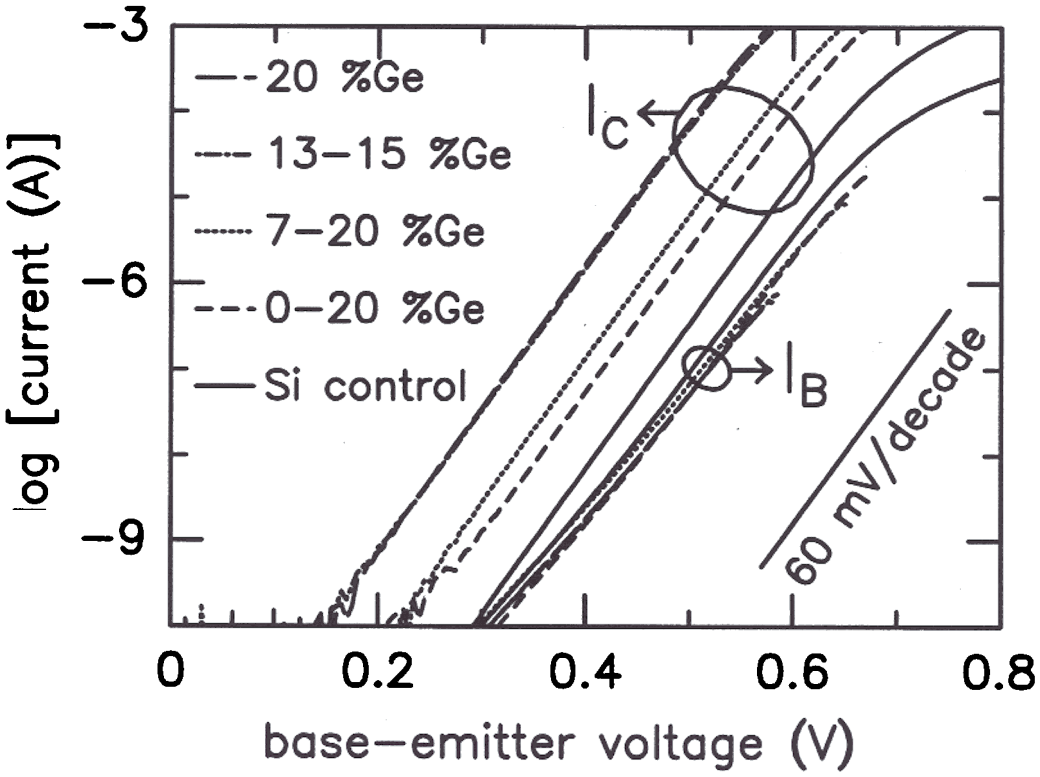


Figure 4.5: Base and collector currents vs. base-emitter voltage (Gummel plots) of the devices of Table 4.1 with an emitter area of $62 \times 62\ \mu m^2$ for zero base-collector reverse bias. Note that the base currents of the devices with *different* base doping and Ge profiles were indistinguishable.

devices, as discussed in Chap. 2.2, if the minority carrier lifetime in the $Si_{1-x}Ge_x$ base layers is sufficiently high. This had previously only been observed in devices grown by UHV-CVD at IBM [69], but not in devices fabricated from layers grown by MBE or non-UHV techniques. The $Si/Si_{1-x}Ge_x/Si$ HBT's fabricated previously with a non-UHV technique, Limited Reaction Processing (LRP), had base currents with slopes of 60 mV/decade (corresponding to an ideality factor η of 1) but which were about 50× larger than the base currents of the silicon control devices [22]. These devices were grown without using a load lock resulting in high oxygen concentrations of about 10^{20} cm^{-3} in the $Si_{1-x}Ge_x$ base layers, and King *et al.* assumed that the abnormally high base currents were due to low minority carrier lifetime in the $Si_{1-x}Ge_x$ material leading to recombination in the narrow gap ($Si_{1-x}Ge_x$) part of the base-emitter depletion region. Our devices had approximately the same effective emitter Gummel number because the emitter implant dose was the same as in Ref. [22], and they had approximately the same base intercept current density $J_{B,0}$ in the Gummel plot as King's silicon control devices. Since in our system the use of a load lock reduced the oxygen concentration in the $Si_{1-x}Ge_x$ layers to below SIMS resolution ($< 10^{18}$ cm^{-3}) and we obtained base currents which were not limited by recombination in the base, it can be inferred that the high oxygen levels in King's devices might indeed have been responsible for the degradation in the minority carrier lifetime observed by King. Other pieces of evidence pointing in this direction are the fact that oxygen incorporated in $Si_{1-x}Ge_x$ layers quenches the band-edge photoluminescence normally observed in our films [96], that in lightly ($\approx 10^{17}$ cm^{-3}) doped $Si_{1-x}Ge_x$ layers grown in our load-locked reactor generation lifetimes of over 1 μs have been observed [97], and that in epitaxially grown *silicon* layers oxygen doping of about 5×10^{19} cm^{-3} has resulted in a dramatically decreased minority carrier lifetime [98].

The collector currents of the devices of Table 4.1 measured at room temperature with zero base-collector reverse bias had an ideal slope of 60 mV/decade, and they

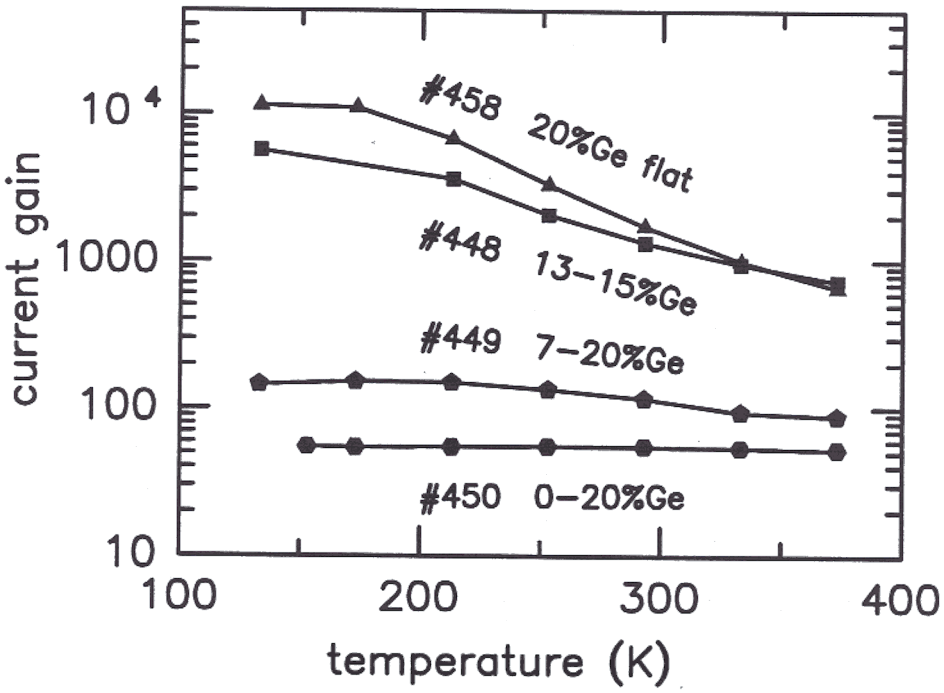


Figure 4.6: Measured maximum current gain vs. temperature for the graded base devices #448, #449, and #450, and for the flat base HBT #458. Note that, unless in a homojunction transistor, low temperature operation in these devices is possible despite the heavily doped emitter.

increased with Ge concentration in the base. Since the base of device #448 was partly compensated by a phosphorus spike as discussed above, its collector current was larger than expected, and we will assume for the modeling in Section 4.5 an effective Ge grading from 13–15% Ge instead of the projected 13–20% Ge. Fig. 4.6 shows the temperature dependence of the maximum common-emitter current gain. In homojunction devices β usually degrades with decreasing temperature because of the bandgap narrowing in the heavily doped emitter which transforms these devices into effective HBT's with *narrow* gap emitter. In our graded base heterojunction devices no gain degradation was observed down to temperatures of 133 K, and the flat base device #458 had a maximum current gain of over 11,000 at 133 K, the highest current

gain ever reported for a silicon-based HBT at cryogenic temperatures.

4.4 Generalized Analytical Model for the Collector Current in HBT's

In this section we shall derive equations for the collector current J_n, the electron concentration in the base $n(x)$, and for the base transit time τ_B of *npn*-HBT's.

Unless in a homojunction *npn*-transistor, where the collector current is limited by drift and diffusion of electrons across the base, hot-electron effects can be important in HBT's. In InP/InGaAs HBT's, for example, as shown in Fig. 4.7, the conduction band spike at the InP/InGaAs emitter-base heterojunction may control the collector current by launching hot electrons into the neutral base with kinetic energies bigger than the conduction band discontinuity ΔE_C, and with mean free paths exceeding the base width. It is currently under discussion whether electrical characteristics of InP/InGaAs HBT's should be interpreted by hot-electron transport or by drift-diffusion [99, 100, 101]. Clearly, if hot electron injection into the base controls collector current the classical drift-diffusion equations which assume quasi-equilibrium are no longer valid.

Since in $Si/Si_{1-x}Ge_x/Si$ HBT's the conduction band discontinuity at the $Si/Si_{1-x}Ge_x$ heterojunction is much smaller than the valence band discontinuity ($\Delta E_C \approx 20$ meV for the $Si/Si_{1-x}Ge_x$ heterojunction), hot electron injection into the base is unlikely. Furthermore, the difference in base transit times obtained by Monte-Carlo simulation and by the drift-diffusion equation of *silicon* bipolar transistors with basewidths as narrow as 200 Å was less than 20% [102]. We therefore assume that the collector current in our $Si/Si_{1-x}Ge_x/Si$ HBT's is limited by transport of electrons through the base by drift and diffusion, and that hot-electron effects can be neglected.

The following derivation is conceptually similar to the diffusion theory for metal-

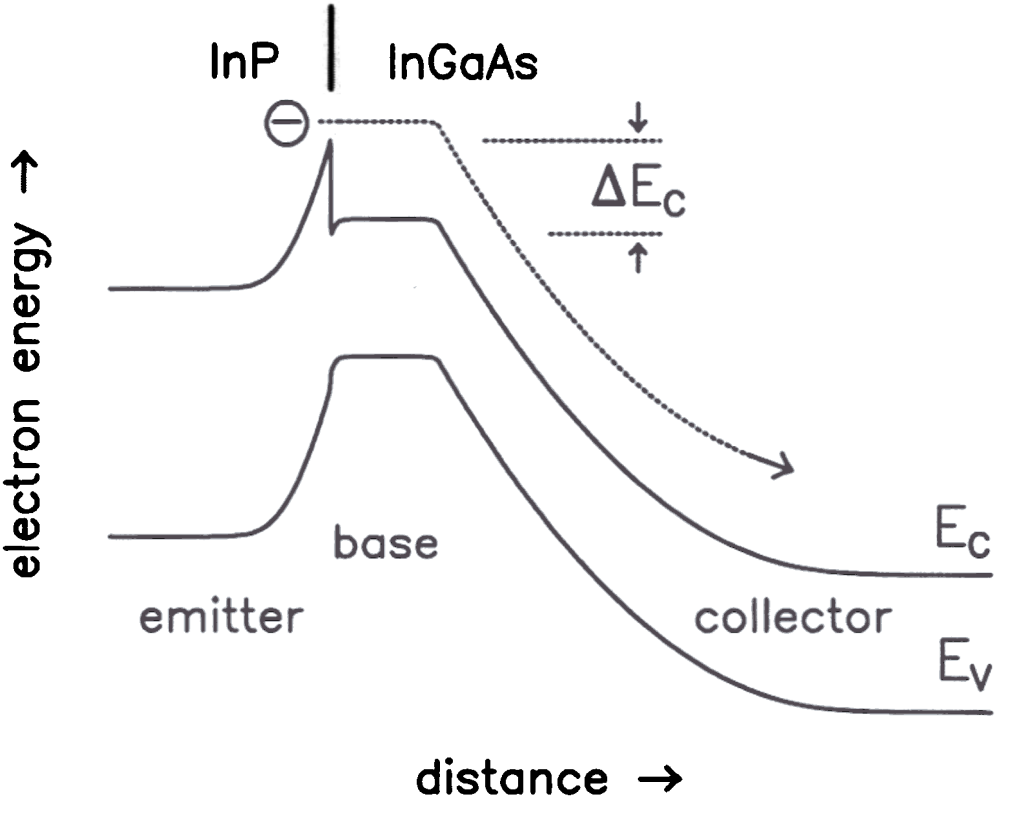


Figure 4.7: Schematic band diagram of InP/InGaAs heterojunction bipolar transistor. Because of the large conduction band discontinuity of the InP/InGaAs heterojunction, electrons enter the InGaAs base with excess kinetic energy and, if the basewidth is smaller than the electron mean free path, reach the collector without scattering in the base.

semiconductor barriers by Schottky, except that the collector current in a HBT is carried by minority carriers, while the current across a Schottky-barrier is carried by majority carriers [103]. For homojunction bipolar transistors, a similar analysis was carried out by Gummel, leading to the famous Gummel-Poon model, where it was shown that the collector current is inversely proportional to the integrated majority carrier (hole) charge in the base [104, 105]. In a HBT this is no longer true because not only the base doping but also the base bandgap determines the height and shape of the potential barrier in the base seen by the electrons. This has been recognized by Kroemer, who derived an expression for the collector current in a graded-base HBT, assuming that the base consists of a charge-neutral region with a constant hole quasi-Fermi level [106]. His expression can explain the experimental results of this chapter if the effect of the strain in the $Si_{1-x}Ge_x$ layer on the effective densities of states N_C and N_V is accounted for (see Section 4.5).

Since in Sections 5.5 and 7.4 we shall encounter bipolar transistors in which the hole quasi-Fermi level in the base is *not* constant, we shall now derive a more general expression for the collector current in a HBT and later show that Kroemer's equation is a special case of our expression. Our derivation also generalizes the results of Ref. [107] obtained for AlGaAs/GaAs HBT's with abrupt heterojunctions.

Consider the transport equations for electrons and holes of Table 4.2 [108]. If the carrier concentrations are known, the electrostatic potential $\Psi(x)$ can be calculated from Poisson's Equation. The energy E_{vac} of an electron brought from a position inside the semiconductor into vacuum is closely related to Ψ ($q\Psi = -E_{vac} + const.$). The electron and hole currents J_n and J_p include the usual drift and diffusion currents. In a semiconductor heterostructure, however, there are additional drift components because the carriers see quasi-electric fields if the electron affinity $\chi = E_{vac} - E_C$ or the bandgap E_G change with distance, as shown in Figs. 4.8 and 4.9. These components are proportional to the gradients of the conduction and valence band discontinuities

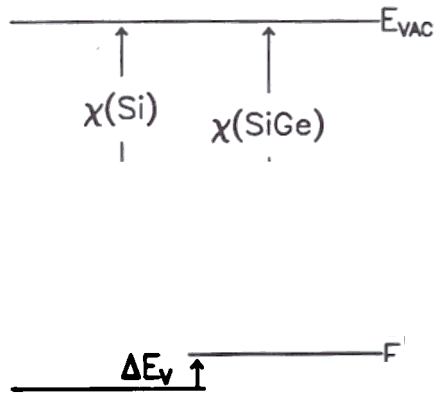


Figure 4.8: Schematic diagram showing the band lineup at the n-Si/p-$Si_{1-x}Ge_x$ heterojunction in the "flatband" condition, i.e. with an applied voltage V_{APP} which just balances the built-in voltage V_{BI} (not to scale). Also shown are definitions of the vacuum energy E_{vac} of electrons, the electron affinity $\chi = E_{vac} - E_C$, the conduction and valence band discontinuities ΔE_C and ΔE_V, and the quasi-Fermi levels Φ_n and Φ_p.

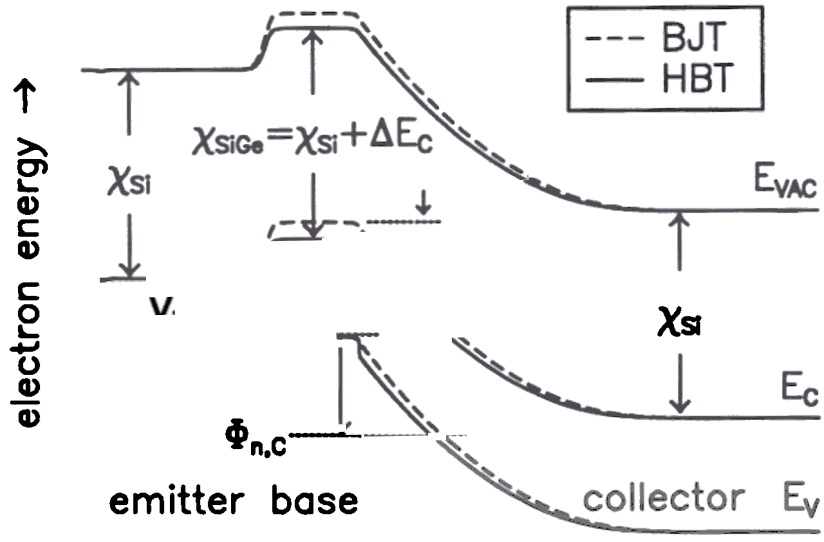


Figure 4.9: Schematic band diagrams of homojunction (dashed lines) and heterojunction (solid lines) bipolar transistor. The electron quasi-Fermi levels in emitter ($\Phi_{n,E}$) and collector ($\Phi_{n,C}$) are separated from the hole quasi-Fermi level in the base ($\Phi_{p,B}$) by the applied voltages V_{BE} and V_{CB}.

Table 4.2: Semiconductor device equations for heterostructures.

Poisson's Equation:

$$\frac{d^2\Psi}{} = -\frac{q}{\epsilon_0\epsilon_S}\left(p - n + N_D{}^+ - N_A{}^-\right) - \frac{1}{\epsilon_S}\frac{\partial\epsilon_S}{\partial x}\frac{\partial\Psi}{\partial x}$$

Continuity Equations for Electrons and Holes:

$$\frac{\partial n}{\partial t} = G_n - U_n + \frac{1}{q}\frac{\partial J_n}{\partial x}$$

$$\frac{\partial p}{\partial t} = G_p - U_p - \frac{1}{q}\frac{\partial J_p}{\partial x}$$

Drift-Diffusion Equations for Electrons and Holes

$$J_n = q\mu_n n\left(\frac{d\Psi}{dx} - \frac{1}{q}\frac{d\Delta E_C}{dx}\right) + qD_n\left(\frac{dn}{dx} - \frac{n}{N_C}\frac{dN_C}{dx}\right)$$

$$J_p = q\mu_p p\left(+\frac{d\Psi}{dx} - \frac{1}{q}\frac{d\Delta E_V}{dx}\right) + qD_p\left(\frac{dp}{dx} - \frac{p}{N_V}\frac{dN_V}{dx}\right)$$

ΔE_C and ΔE_V, as can be seen in Eqns. 4.4 and 4.5. If the effective densities of states N_C and N_V change with distance, an additional diffusion term arises

In a homojunction bipolar transistor the collector current can be related to $\Psi(x)$ by realizing that it is proportional to the gradient of the electron quasi-Fermi level Φ_n

$$J_n = n\mu_n\frac{d\Phi_n}{dx}$$

where μ_n is the electron mobility. The electron quasi-Fermi level (electrochemical potential) Φ_n includes terms related to the electrostatic potential $\Psi(x)$, the position

of the minimum of the conduction band with respect to the vacuum level (electron affinity χ), and the chemical potential, which is $[k_BT \ln(n/N_C)]$ for Boltzmann statistics. Instead of the electron affinity χ we use the conduction band discontinuity ΔE_C with respect to silicon to describe the position of the conduction band with respect to the vacuum level, and we use the "+"-sign for ΔE_C if the conduction band is *lowered* with respect to the one of silicon, like in the Type-I band lineup of the heterojunction between silicon and the strained $Si_{1-x}Ge_x$ alloy. With these assumptions, Eqn. 4.6 and a similar equation for the hole current J_p can be derived as shown in Table 4.2 [108].

We now neglect generation of electron-hole pairs and avalanche in the reverse-biased base-collector junction, recombination in the forward-biased base-emitter junction, hot-electron effects, and high-level injection into the base ($G_n = U_n = G_p = U_p = 0$). For the calculation of the electrostatic potential $\Psi(x)$ from Eqn. 4.1 we assume, that the hole current J_p is much smaller than the electron current J_n; and, generalizing Kroemer's derivation, that the base consists of *several* charge-neutral layers. There can be depletion and accumulation regions in between the charge-neutral p-layers, or between the p-base and the n-type emitter and collector. This is important if depleted regions instead of charge-neutral regions control collector current, as will be encountered in Section 5.5. Since the hole current is negligible, the hole quasi-Fermi level *in each neutral p-layer* is constant In a HBT, the charge-neutral p-layers are all connected to the base terminal, but in Chap. 7 we shall encounter a case where two charge-neutral p-type layers are connected to separate base contacts, resulting in *different* hole quasi-Fermi levels in the two base layers. The emitter and collector terminals are connected to the charge-neutral n-type emitter and collector layers, respectively.

We now replace the electron mobility μ_n in Eqn. 4.4 by the electron diffusion coefficient using Einstein's Equation ($D_n = \frac{k_BT}{q} \mu_n$), and replace the term describing

the conduction band density of states gradient, dN_C/dx, by the logarithmic derivative:

$$\frac{n}{N_C}\frac{dN_C}{dx} = n\,\frac{d\,\ln(N_C)}{dx}$$

and get

$$J_n = -\frac{q^2}{k_BT}\,D_n\,n\,\frac{d}{dx}\left(\Psi + \frac{1}{q}\,\Delta E_C + \frac{k_BT}{q}\,\ln(N_C)\right) + qD_n\,\frac{dn}{dx}$$

This equation can be integrated using the integrating factor

$$\exp\left\{\frac{q}{k_BT}\left(\Psi + \frac{1}{q}\,\Delta E_C + \frac{k_BT}{q}\,\ln(N_C)\right)\right\}$$

Since J_n is assumed constant (no hole or generation-recombination current) we can write (assuming that D_n is a function of x):

$$J_n \int_{x_B}^{x_C} \frac{1}{D_n}\,\exp\left\{\frac{q}{k_BT}\left(\Psi + \frac{1}{q}\,\Delta E_C + \frac{k_BT}{q}\,\ln(N_C)\right)\right\}\,dx$$

$$\left[q\,n(x)\,\exp\left\{\frac{q}{k_BT}\left(\Psi + \frac{1}{q}\,\Delta E_C + \frac{k_BT}{q}\,\ln(N_C)\right)\right\}\right]_{x_B}^{x_C} \qquad (4.10)$$

where the integral is taken from a point x_E in the neutral emitter to a point x_C in the neutral collector.

For the electrostatic potential we use the constant hole quasi-Fermi levels Φ_p in one of the neutral p-type base layers as a reference. For a HBT, where all the neutral p-type base layers are shorted to each other, the electrostatic potentials in the neutral n-emitter and n-collector are then:

$$\Psi(x_E) = \frac{k_BT}{q}\,\ln\left(\frac{N_{C,E}}{N_{D,E}}\right) \quad V_{BE}$$

$$\Psi(x_C) = \frac{k_BT}{q}\,\ln\left(\frac{N_{C,C}}{N_{D,C}}\right) \quad V_{BC} \qquad (4.11$$

where $N_{C,E}$ and $N_{C,C}$ are the conduction band densities of states, and $N_{D,E}$ and $N_{D,C}$ the doping levels in the emitter and collector, respectively. Inserting $\Psi(x_E)$ and

$\Psi(x_C)$ into Eqn. 4.10 yields the desired equation, linking the collector current to the electrostatic potential $\Psi(x)$ in the base:

$$J_n \quad -\frac{q\ [\exp(qV_{BE}/k_BT) - \exp(qV_{BC}/k_BT)]}{\int_{x_B}^{x_C} \frac{1}{D_n N_C}\ \exp\left\{-\frac{q}{k_BT}\left(\Psi + \frac{1}{q}\,\Delta E_C\right)\right\} dx} \tag{4.12}$$

In this equation, the electron diffusion coefficient D_n, and the conduction band discontinuity ΔE_C and density of states N_C, are known from the device structure as a function of position x. The integral is taken from a point x_E in the neutral emitter to a point x_C in the neutral collector and includes the base-emitter and base-collector space charge regions. This is important, because in some cases the collector current is controlled by the conduction band in a depletion region, as demonstrated in Section 5.5. The electrostatic potential $\Psi(x)$ can be analytically calculated in some important cases using the depletion approximation (see Sections 5.5 and 7.4)

The most important observation in Eqn. 4.12 is that the collector current will be controlled by the region which contributes most to the integral in the denominator which is the region where the conduction band E_C presents the highest barrier for electrons. This can be either a charge-neutral, a depletion, or an accumulation region.

We shall now show how Eqn. 4.12 reduces to Kroemer's equation from Ref. [106]. He assumed that the base consisted of one charge-neutral p-region in which the bandgap varied with position. The potential $\Psi(x)$ in the base corresponding to this case measured with respect to the hole quasi-Fermi level Φ_p is

$$\Psi(x) \quad -E_G(x) + \frac{k_BT}{q}\ln\left(\frac{N_{V,B}}{N_{A,B}}\right) - \frac{1}{q}\,\Delta E_C \tag{4.13}$$

Inserting Eqn. 4.13 into Eqn. 4.12 yields:

$$\mathrm{J_n} \quad = -\frac{q\ [\exp(qV_{BE}/k_BT) - \exp(qV_{BC}/k_BT)]}{\int_{x_E}^{x_C} \frac{1}{D_n N_C}\ \exp\left\{-\frac{q}{k_BT}\left(\Psi(x) + \frac{1}{q}\,\Delta E_C\right)\right\} dx}$$

$$-\frac{q\ [\exp(qV_{BE}/k_BT) - \exp(qV_{BC}/k_BT)]}{\int_{x_B}^{x_C} \frac{1}{D_n}\,\frac{N_A}{N_{C,B}N_{V,B}}\ \exp\left\{-\frac{q}{k_BT}E_G(x)\right\} dx}$$

$$\approx \frac{q\,[\exp(qV_{BE}/k_BT) - \exp(qV_{BC}/k_BT)]}{\int_{x_{BB}}^{x_{BC}} \frac{N_A(x)}{D_n(x)n_i^2(x)}\,dx} \tag{4.14}$$

where the only approximation has been to neglect the effect of the base-emitter and base-collector depletion regions, by replacing x_E and x_C, which are located in the charge-neutral n-regions, by the boundaries of the neutral base, x_{BE} on the emitter and x_{BC} on the collector side. Eqn. 4.14 is Kroemer's result.

In analogy to Kroemer's derivation in Ref. [106], we can also generalize his expressions for the electron concentration in the base $n(x)$ and the base transit time τ_B. We start from Eqn. 4.10, but integrate now from an arbitrary point x in the base to a point x_C in the base-collector space charge region, and solve for $n(x)$:

$$\frac{J_n \int_x^{x_C} \frac{1}{D_n N_C} \exp\left\{-\frac{q}{k_BT}\left(\Psi + \frac{1}{q}\,\Delta E_C\right)\right\} dx}{\left[\frac{q}{N_C} \exp\left\{-\frac{q}{k_BT}\left(\Psi + \frac{1}{q}\,\Delta E_C\right)\right\}\right]_x} \tag{4.15}$$

where the contribution from the collector space charge region can be neglected. From Eqn. 4.15 the base transit time can be calculated:

$$\tau_B \qquad \frac{Q_B}{J_n} = -\frac{q}{J_n} \int_{x_{BB}}^{x_{BC}} n(x)\,dx \tag{4.16}$$

where Q_B is the part of the hole charge Q_{EC} entering the input (base) terminal which neutralizes the minority carriers in the base. Q_{EC} is the total hole charge necessary to control the output (collector) current J_n. The integration of Eqn. 4.16, therefore, covers all electrons in the base which have to be neutralized by holes entering from the base terminal. With Eqn. 4.15, the expression for τ_B becomes:

$$\tau_B \quad \int_{x_{BB}}^{x_{BC}} \left[N_C(x) \exp\left\{ \frac{q}{k_BT}\left(\Psi(x) + \frac{1}{q}\,\Delta E_C(x)\right)\right\} \times \right.$$

$$\left. \times \int^{x_{BC}} \frac{1}{D_n(z)N_C(z)} \exp\left\{ \frac{q}{k_BT}\left(\Psi(z) + \frac{1}{q}\,\Delta E_C(z)\right)\right\} dz \right] dx \tag{4.17}$$

Comparison of Analytical Model and Experiment

We now use Kroemer's Equation to model our experimental data from Section 4.3. It can be physically understood by considering that the height of the conduction band barrier in the base E_C with respect to the quasi-Fermi level Φ_p is equal for p-type $Si_{1-x}Ge_x$ and p-type silicon doped $\left\{N_A(Si)\ e^{-\Delta E_G/k_BT}\right\}$, where ΔE_G is the bandgap reduction in the strained $Si_{1-x}Ge_x$ layer compared to Si, and *equal* effective densities of states N_C and N_V have been assumed for silicon and $Si_{1-x}Ge_x$ (see Fig. 4.1). Neglecting differences in mobilities, one can then model the HBT by "transforming" it into a silicon homojunction transistor with an effective Gummel number $N_{G,eff}$, which could be inserted into the corresponding expression for homojunction transistors (Gummel's result) [104]

$$J_C = \frac{qD_n n_i^2}{N_G}\ e^{qV_{BE}/k_BT} \tag{4.18}$$

where N_G is the *Gummel number*,

$$N_G = \int_{neutral\ base} N_A(x)\ dx$$

and

$$N_{G,eff} = \int_{base} N_A(x)\ e^{-\Delta E_G(x)/k_BT}\ dx = \int_{base} \frac{n_i^2(Si)}{n_i^2(SiGe)}\ N_A(x)\ dx \tag{4.19}$$

Eqn. 4.19 can be evaluated analytically for the case of linear grading and constant doping N_A

$$N_{G,eff} = \frac{W_B\ N_A\ k_BT}{\Delta E_{G,2} - \Delta E_{G,1}}\ e^{-\Delta E_{G,1}/k_BT}\left(1 \quad e^{-(\Delta E_{G,2} - \Delta E_{G,1})/k_BT}\right) \tag{4.20}$$

where W_B is the neutral base width and $\Delta E_{G,1}$ and $\Delta E_{G,2}$ are the minimum and maximum bandgap reductions compared to silicon.

For a $Si_{1-x}Ge_x$ base, Eqn. 4.19 has to be modified because the strain affects the band structure, as shown in Fig. 4.10. In the presence of compressive strain in the

$Si_{1-x}Ge_x$ alloy, the six-fold degenerate conduction band minima of silicon along the {100} directions are split into energetically lower lying four-fold degenerate bands in the growth plane and two-fold degenerate bands perpendicular to the growth plane in the strained $Si_{1-x}Ge_x$ alloy. This splitting is taken from the calculations of van de Walle [32]. The degeneracy between the light and heavy hole band is also removed by the strain. As a result of the band splitting in strained $Si_{1-x}Ge_x$ the electron (hole) density in the energetically higher (lower) lying conduction (valence) band is decreased by a Boltzmann factor $\exp(\Delta E/k_BT)$ resulting in fewer electrons and holes available for transport. Since the collector current in a HBT is proportional to ${n_i}^2 \propto N_C N_V(SiGe)$ for a given bandgap, taking the reduced effective densities of states into account lowers the calculated collector current by the temperature dependent factor $N_C N_V(SiGe)/N_C N_V(Si)$ shown in Fig. 4.11:

$$N_{G,eff} = \int_{base} \frac{{n_i}^2(Si)}{{n_i}^2(SiGe)} N_A(x)\, dx$$

$$\int_{base} \frac{N_C N_V(Si)}{N_C N_V(SiGe)} N_A(x)\, e^{-\Delta E_G(x)/k_BT}\, dx \qquad (4.21)$$

Using Eqn. 4.21 and the target growth parameters of Table 4.1 (except for 13–15% Ge grading of device #448, as discussed above) the collector current enhancement of the $Si_{1-x}Ge_x$ devices over a silicon control device predicted by this model is plotted vs. temperature in Fig. 4.12 together with experimental data taken in the temperature range between 143 and 373 K. The experimental results were corrected for differences in the Gummel numbers by normalizing the collector current by the base sheet resistance $R_{B,sh}$ measured at room temperature. The temperature dependent $N_C N_V$ ratio shown in Fig. 4.11 was included. No parameters were adjusted.

The deviations of the model predictions from the experimental data might be due to uncertainties in the Ge concentrations of about 1% Ge, shown with dashed lines in Fig. 4.12, and to mobility differences between Si and strained $Si_{1-x}Ge_x$ which have

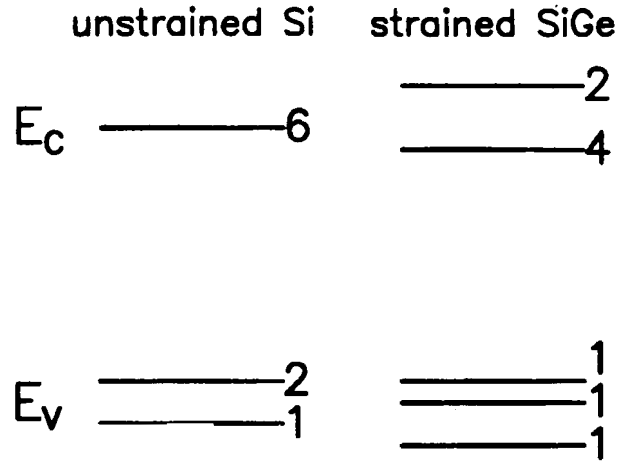


Figure 4.10: Compressive strain in the $Si_{1-x}Ge_x$ base removes the six-fold degeneracy of the conduction band and the two-fold degeneracy of the valence band (light and heavy hole). As a consequence, the effective densities of states for electrons and holes decrease with increasing strain.

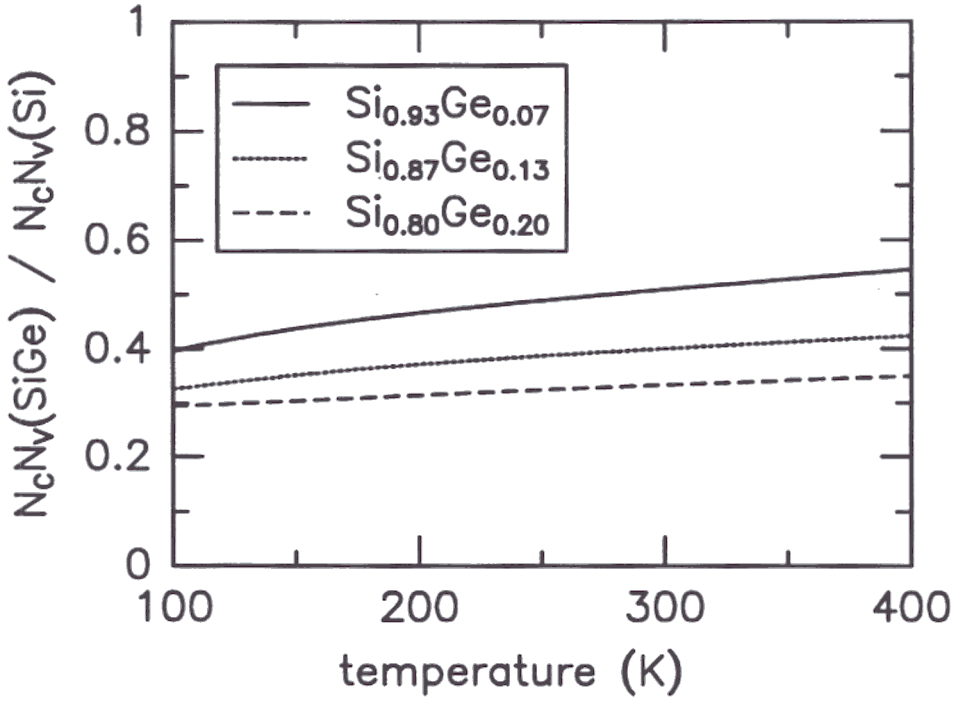


Figure 4.11: Calculated reduction of effective density of states product $N_C N_V$ for the $Si_{1-x}Ge_x$ base of a HBT under compressive strain. The collector current is accordingly reduced.

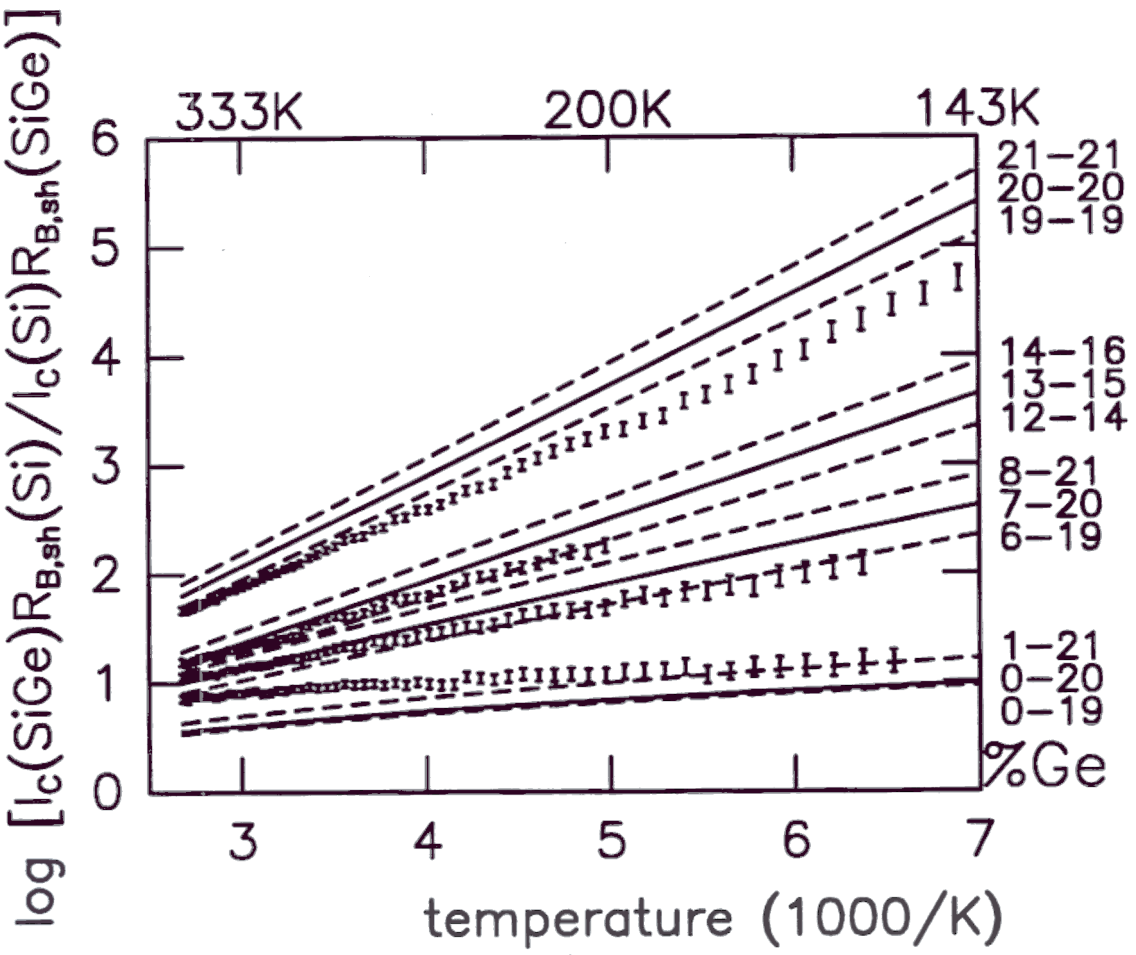


Figure 4.12: Temperature dependence of the measured collector current enhancement of the various $Si/Si_{1-x}Ge_x/Si$ HBT's over a silicon control device, corrected for base sheet resistance differences (error bars). Also shown are calculations (solid and dashed lines) taking into account the reduction in the $N_C N_V$ product. The solid lines correspond to the Ge concentrations expected from the growth parameters, except for the 13–15% Ge device, as explained in the text. The dashed lines are calculations for $\Delta x = \pm 1\%$ Ge concentration to show the sensitivity of the normalized collector current to Ge concentration.

not yet been determined. The agreement for the graded base devices is good, taking into account that the collector current is very sensitive to the Ge concentration at the edge of the base-emitter depletion region in the base (this region presents the highest barrier for electrons and therefore controls the collector current). The collector current enhancement in the flat base HBT is slightly less than that expected for a $Si_{0.80}Ge_{0.20}$ base with a ΔE_G of 168 meV, which could be due to base dopant outdiffusion from the $Si_{1-x}Ge_x$ base into the silicon collector as outlined in Chapter 5 (device #458 had no intrinsic $Si_{1-x}Ge_x$ spacer layers which would alleviate the deleterious effects of base dopant outdiffusion). The comparison of the measured collector current enhancement and Kroemer's simple theory, modified to include the strain-induced reduction of the $N_C N_V$ product in the $Si_{1-x}Ge_x$ layers, shows the excellent control of RTCVD for graded $Si_{1-x}Ge_x$ base profiles.

Chapter 5

Base Dopant Outdiffusion Effects in $Si/Si_{1-x}Ge_x/Si$ HBT's

5.1 Introduction

In this chapter we demonstrate that small amounts of boron outdiffusion from heavily doped $Si_{1-x}Ge_x$ bases into Si emitter and collector cause parasitic barriers in the conduction band which drastically reduce the collector current enhancement in the HBT's.

We then show that undoped intrinsic $Si_{1-x}Ge_x$ spacer layers on both sides of the base can remove the parasitic barriers resulting in a strongly improved collector current [109, 110]. The concept of an intrinsic spacer at the base-emitter junction to compensate for dopant diffusion has previously been reported in AlGaAs/GaAs HBT's by Malik *et al.* but the effects of base dopant outdiffusion were not investigated in detail [111].

Recently, our work has been extended by Pruijmboom *et al.* and Slotboom *et al.* by demonstrating the deleterious effect of parasitic potential barriers on the high frequency performance of $Si/Si_{1-x}Ge_x/Si$ HBT's [71, 112].

We first consider computer simulations showing the effects of dopant outdiffusion and intrinsic $Si_{1-x}Ge_x$ spacer layers. Then electrical measurements on HBT's with

thin, heavily doped bases are described. Finally, an analytical model for describing the parasitic barriers is developed.

5.2 Parasitic Potential Barriers Caused by Base Dopant Outdiffusion

As outlined in Chap. 2.3, narrow, heavily doped bases are desired for circuit applications of $Si/Si_{1-x}Ge_x/Si$ HBT's. These structures can be grown by various techniques; the final doping and Ge profiles, however, are strongly dependent on the thermal budget employed during device fabrication. To evaluate the effect of boron diffusion on the electrical characteristics of $Si/Si_{1-x}Ge_x/Si$ HBT's, we consider a flat-base HBT with a base doping of 10^{19} cm^{-3} and a base Ge concentration of 20%. An exponentially decreasing boron outdiffusion tail extends from the $Si_{1-x}Ge_x/Si$ interface into the Si collector which is doped 10^{17} cm^{-3} ($N_A(x) \propto e^{-|x-L|/L_D}$, where L is the position of the SiGe/Si heterojunction).

This vertical profile is input into a one-dimensional drift-diffusion solver (SEDAN) [113], modified to incorporate $Si/Si_{1-x}Ge_x$ heterojunctions using the values of conduction and valence-band discontinuities calculated by People and Bean [30]. Fig. 5.1 shows for several values of L_D the calculated conduction and valence bands close to the base-collector junction and the minority carrier (electron) concentration in the base. Note that for no outdiffusion *both* sides of the $Si/Si_{1-x}Ge_x$ heterojunction are depleted and that the conduction band spike therefore does not limit the collector current. Outdiffusion of boron into the Si collector results in the formation of parasitic potential barriers for electrons in the conduction band. Even small amounts of boron outdiffusion ($L_D \approx 30$ Å) cause large parasitic barriers for electrons at the base-collector junction (barrier height $\Psi_0 \approx 85$ meV). These barriers will significantly impede the flow of electrons from emitter through the base to the collector, thereby

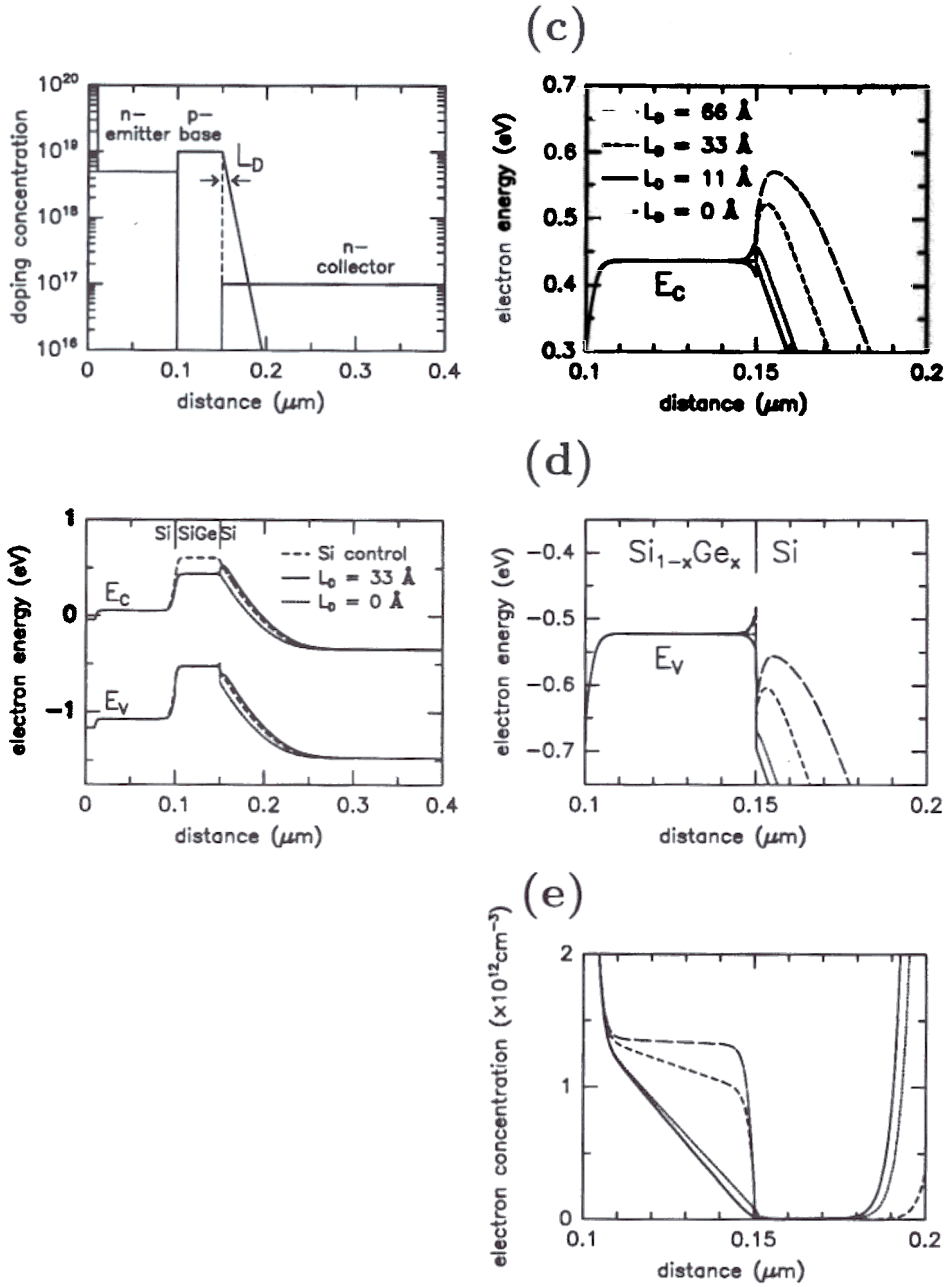


Figure 5.1: Simulation of band diagram and electron concentration for a $Si/Si_{1-x}Ge_x/Si$ HBT with the doping profile of (a). Note the exponential dopant outdiffusion tail (diffusion length L_D) into the Si collector region. The band diagram (b) shows the parasitic conduction band barrier at the $Si_{1-x}Ge_x/Si$ interface. (c) and (d) show conduction and valence band, respectively, at the base-collector junction for various diffusion lengths L_D. (e) The parasitic conduction band barrier causes a deviation from the triangular electron profile in the base leading to increased minority carrier charge storage in the base even as I_C decreases.

degrading the collector current enhancement possible with the $Si_{1-x}Ge_x$ alloy. Note that the overall barrier for holes traveling from base to emitter (one component of the base current) is unchanged.

For an L_D of 33 Å the $Si_{1-x}Ge_x$ side of the $Si_{1-x}Ge_x$/Si heterojunction is in an *accumulation* region and the Si side in a *depletion* region formed by the depletion regions of the heterojunction and the *p-n* junction which touch each other. For this case the parasitic barrier in the conduction band is fully contained in a depletion region. For an L_D much bigger than 66 Å there is a charge-neutral *p*-Si region between the depletion regions of the heterojunction and the *p-n* junction (not shown in Fig. 5.1). In this case the highest potential barrier seen by the electrons in the base has the same height as in a homojunction device.

The parasitic barriers caused by even small amounts of dopant outdiffusion or non-abrupt interfaces degrade device performance by reducing the collector current and therefore the current gain improvement possible in the HBT's, as shown in Fig. 5.2 where the simulated normalized collector current is plotted logarithmically vs. inverse temperature for the band diagrams of Fig. 5.1. For example, for an L_D of only 33 Å there is already a 3.4× reduction of the collector current at room temperature.

Parasitic barriers also increase the base transit time τ_B, by causing increased minority carrier charge storage in the base as shown in Fig. 5.1(e). In their presence, the ideal triangular electron profile characteristic for a constant doping concentration and bandgap in the base is replaced by a trapezoidal profile resulting in an increase in $\tau_B = Q_B/I_C$ because of the increased electron charge Q_B and the decreased collector current I_C. This effect was first experimentally observed by Pruijmboom *et al.* in high-frequency measurements of Si/$Si_{1-x}Ge_x$/Si HBT's [71].

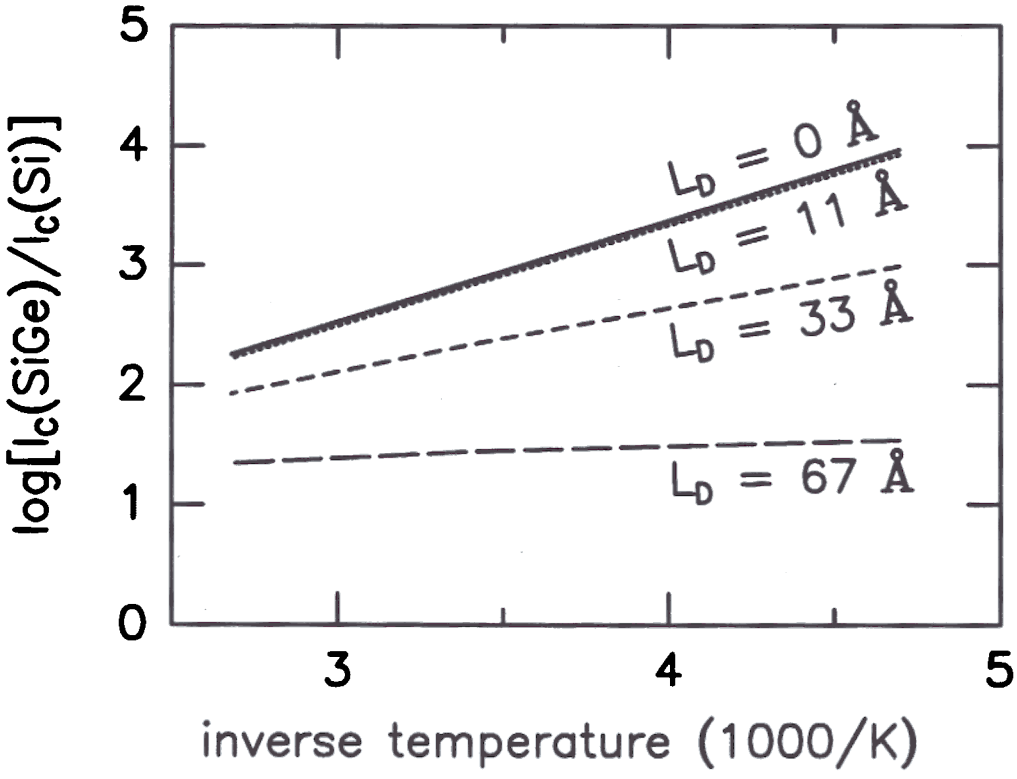


Figure 5.2: Simulation of normalized collector current vs. inverse temperature (Arrhenius plot) for various values of L_D.

5.3 The Concept of Undoped $Si_{1-x}Ge_x$ Spacer Layers

The deleterious effect of base dopant outdiffusion from the $Si_{1-x}Ge_x$ base into silicon emitter and collector can be counteracted by inserting intrinsic $Si_{1-x}Ge_x$ layers on both sides of the base [109]. These spacers have to be wide enough to contain the boron outdiffusion tails resulting from the thermal budget of the process. They increase, however, the width of the strained $Si_{1-x}Ge_x$ layer making the structure more likely to relax by incorporating misfit dislocations at the heterointerface.

We now consider the device structure of Fig. 5.3 with a base doping of 5×10^{19} cm^{-3}, a base width of 300 Å and Ge concentration of 18%, leading to a base sheet resistance of about 800 $\Omega/\square$. The collector doping is chosen in the 10^{17} cm^{-3} range based on the tradeoff between breakdown voltage BV_{CEO} (requiring a low collector doping level) and onset of high-level injection in the collector (Kirk effect) [114, 115]. If the base is doped above 2×10^{18} cm^{-3} a lightly doped n-Si spacer has to be inserted between base and emitter to prevent tunneling leakage in the base-emitter junction [81]. Usually, advanced bipolar IC processes employ a heavily doped polysilicon emitter to allow self-aligned emitter and base contacts [3]. The formation of the polysilicon emitter contributes significantly to the thermal budget of the IC process.

To illustrate how the thermal budget of the process affects the performance of the $Si/Si_{1-x}Ge_x/Si$ HBT of Fig. 5.3, a computer simulation is considered. First, the vertical profile is calculated using the process simulation program SUPREM III for various thermal budgets, assuming that the diffusion coefficients of boron in $Si_{1-x}Ge_x$ and Si are equal and that there is no segregation of boron at the $Si/Si_{1-x}Ge_x$ interface. Recent work indicates that boron tends to segregate into the $Si_{1-x}Ge_x$ and that boron diffusion in $Si_{1-x}Ge_x$ is less severe than in silicon [116, 117]. Taking these results into consideration, the simulation presented here represents a worst case scenario.

The vertical profile from SUPREM III is then input into the drift-diffusion solver

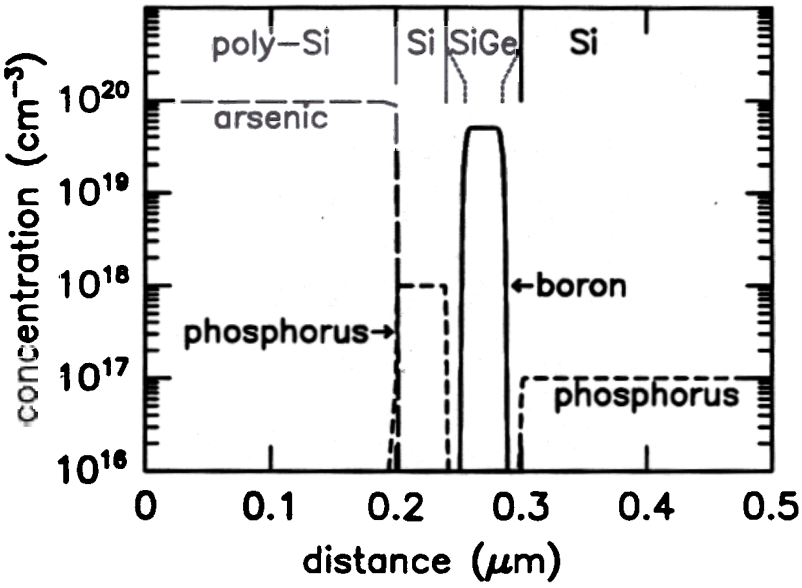


Figure 5.3: Doping profile of HBT structure with a base sheet resistance of approximately 800 Ω/□.

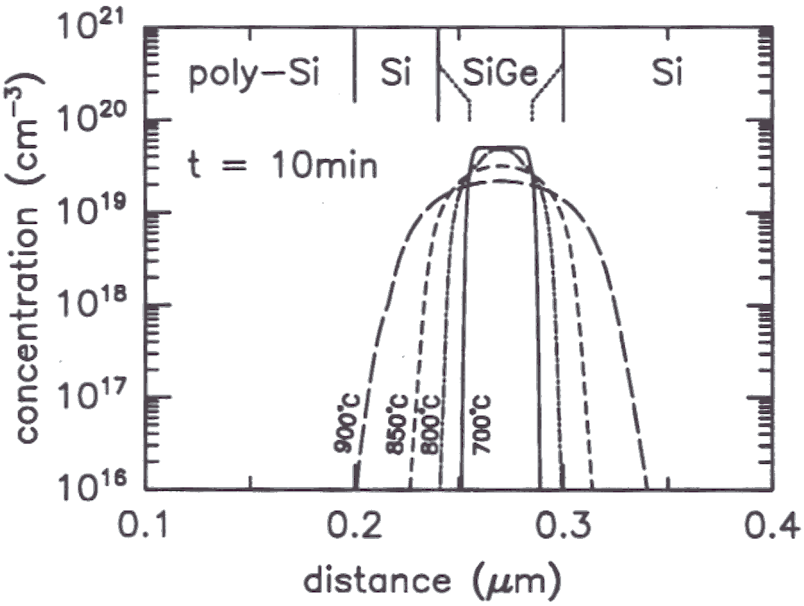


Figure 5.4: Simulated boron doping profile (SUPREM III) for various anneals. If the $Si_{1-x}Ge_x$ layer thickness is increased by adding 150 Å thick intrinsic $Si_{1-x}Ge_x$ spacer layers on both sides of the base, the diffused boron profile is still contained inside the $Si_{1-x}Ge_x$ layer for temperatures below 850°C.

SEDAN. Fig. 5.4 shows calculated doping profiles for a 10 min anneal at various temperatures, and Fig. 5.5 the corresponding band diagrams for a structure (a) without, and (b) with 150 Å thick spacers. Note the absence of parasitic barriers in the device with spacers up to annealing temperatures of 850°C. Fig. 5.6 shows the simulated collector current density at a fixed base-emitter bias as a function of anneal temperature. Increasing the thermal budget of the process leads to a strong degradation of the collector current. If spacers on both sides of the base are employed, however, 10 min anneals up to 850°C do not result in the formation of parasitic electron barriers because the boron diffuses into the $Si_{1-x}Ge_x$ spacer layers instead of silicon. The intrinsic spacers, therefore, improve substantially the tolerance of the device structure for the thermal budget of the process.

These simulations show that in the design of a $Si/Si_{1-x}Ge_x/Si$ HBT process intrinsic $Si_{1-x}Ge_x$ spacer layers on both sides of the base should be considered according to the thermal budget of the process. The critical thickness limitation of the strained $Si_{1-x}Ge_x$ layer, however, limits the improvement which can be obtained for flat-base devices, given the thermal budget of the process.

5.4 Experimental Observation of Base Dopant Outdiffusion Effects

$Si/Si_{0.80}Ge_{0.20}/Si$ transistor structures were grown and processed as described in Chap. 3. Transmission electron microscopy on similar structures with a Ge concentration in the base of 20% showed a negligible number of misfit dislocations (spacing greater than 10 μm); we conclude therefore that these base layers were strained. In one of the device structures (#457) nominally undoped 80 Å thick $Si_{1-x}Ge_x$ spacer layers were added on both sides of the base, as shown in Table 5.1. In all other devices no spacers were inserted so that the p-n junction after the growth of the base

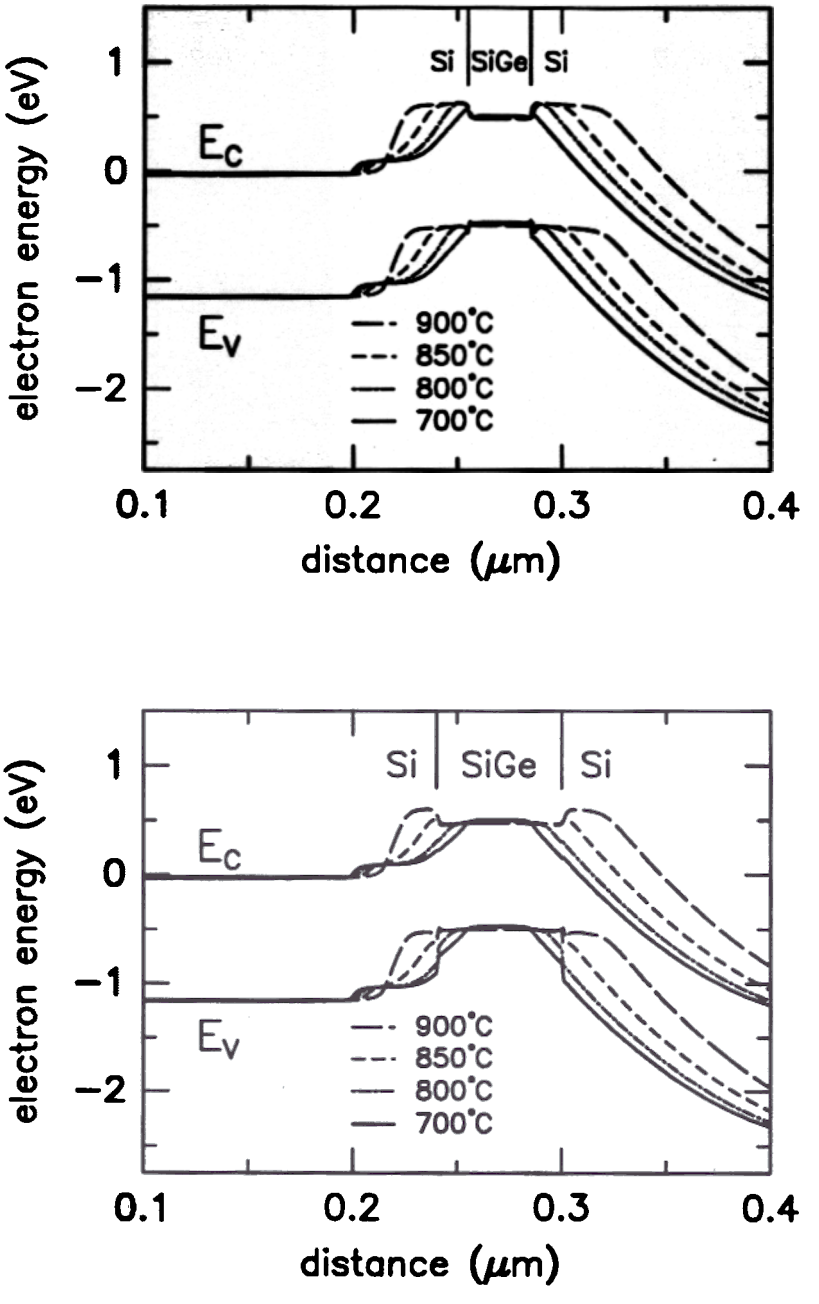


Figure 5.5: Simulated band diagrams for various 10 min anneals for a structure (a) without, and (b) with 150 Å thick spacers.

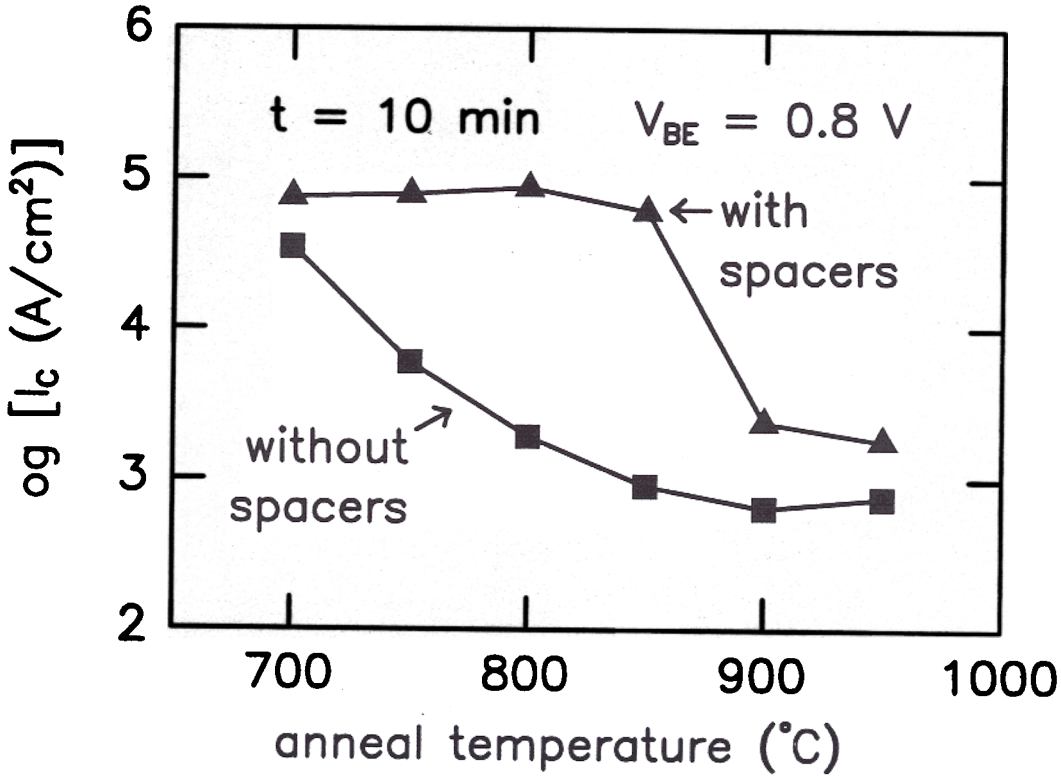


Figure 5.6: Simulated collector current vs. annealing temperature showing the degradation of the collector current with increasing anneal temperature and the improved performance of devices with $Si_{1-x}Ge_x$ spacers

Table 5.1: Parameters of test transistor structures discussed in Section 5.4. The error bars of the activation energies E_A of the Arrhenius plots are about 10 meV

device #	246	633	457	458	460
%Ge	0	0	20	20	20
nom. base doping (cm^{-3})	10^{19}	10^{19}	10^{20}	5.5×10^{18}	10^{20}
doped base width (Å)	824	600	120	250	280
$R_{B,sh}$ ($k\Omega/\square$)	2.1	3.6	2.1	12.0	0.8
spacer thickness (Å)	0	0	80	0	0
measured E_A (meV)	0	0	73	142	-3

coincided with the $Si/Si_{1-x}Ge_x$ heterojunction Note that the base sheet resistance of the silicon control device #246 was much lower than the corresponding value of the flat-base HBT #458 despite the similar doping, because the silicon control device had a wider base. The thermal budget of the process consisted of the emitter growth at 850°C for 3 min and the implant anneal at 800°C for 10 min, and we shall demonstrate now that this thermal budget caused a degradation of the performance of the heavily doped devices.

In a flat-base HBT in which no base dopant outdiffusion has occurred, the ratio of collector current and base sheet resistance should reflect the increased emitter injection efficiency compared to a silicon control device (see Eqns. 2.7 and 4.21):

$$\frac{I_C}{R_{B,sh}} = q^2 A_e \, \mu_p \, D_n \, {n_i}^2(Si) \, \frac{N_C N_V(SiGe)}{N_C N_V(Si)} \, e^{\Delta E_G/k_B T} \, e^{qV_{BE}/k_B T} \qquad (5.1)$$

where A_e is the emitter area, μ_p the in-plane hole mobility in the $Si_{1-x}Ge_x$ base, D_n the electron diffusion coefficient, $N_C N_V$ the effective density of states product, and the pinched base resistance $R_{B,sh}$ is given by Eqn. 2.7. This ratio is shown in Fig. 5.7 for the devices of Table 5.1. Device #458 which was doped 5.5×10^{18} cm^{-3}

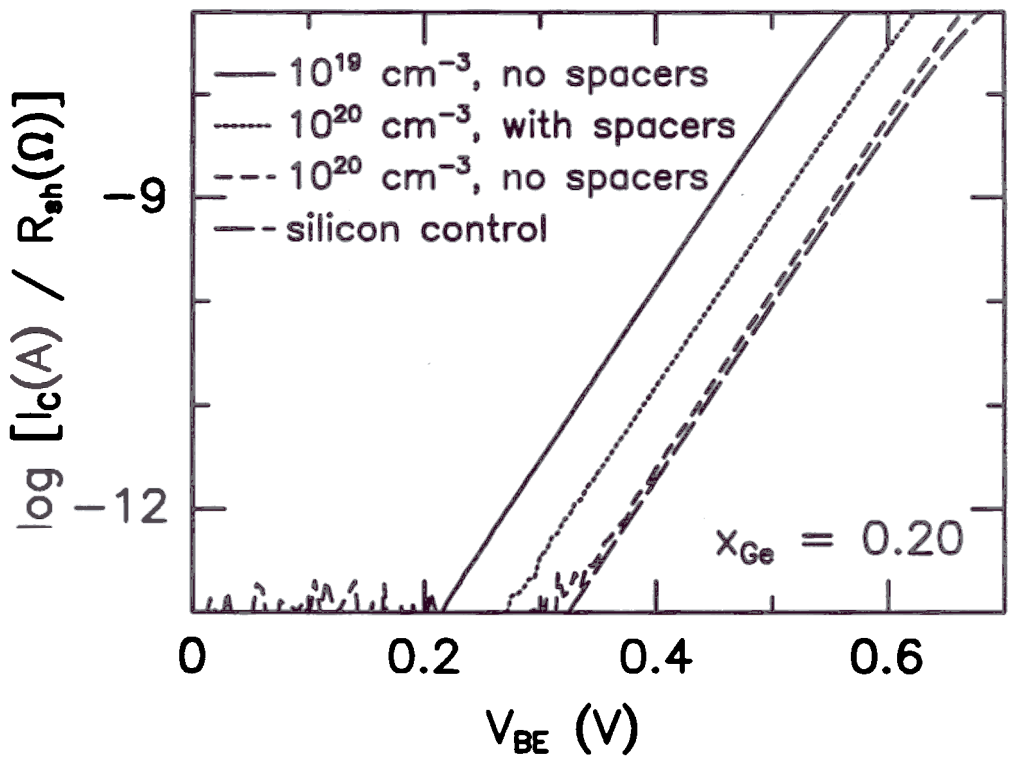


Figure 5.7: Ratio of collector current and base sheet resistance vs. base-emitter voltage for devices #457, #458, #460, and the silicon control device #633, showing the collector current degradation resulting from dopant outdiffusion. All devices had an emitter area of 62×62 μm^2.

had a 80× larger $I_C/R_{B,sh}$ than the silicon control #633, compared to ×10 and ×1.5 improvements of the devices #457 and #460 doped 10^{20} cm^{-3} with and without spacers, respectively.

To prove that the degradation of the collector current was indeed due to parasitic barriers, temperature dependent current-voltage measurements were performed and evaluated as in Ref. [22] (see Fig. 5.8). If the ratio of the collector currents of a $Si/Si_{1-x}Ge_x/Si$ HBT (without dopant outdiffusion) and a silicon control device with the same base doping is plotted logarithmically vs. inverse temperature (Arrhenius plot), the activation energy E_A, proportional to the slope of the Arrhenius plot, should correspond to the bandgap difference ΔE_G between silicon and the strained $Si_{1-x}Ge_x$ base (see Eqn. 2.2). We shall prove in Section 5.5 that Eqn. 2.2 cannot be used to describe the degraded normalized collector current curves of Fig. 5.8.

Fig. 5.8 and the fitted values of E_A in Table 5.1 show, however, that the activation energy E_A for the devices doped 10^{20} cm^{-3} is significantly smaller than the ideal value of 168 meV expected for ΔE_G of a $Si_{0.80}Ge_{0.20}$ layer from Ref. [30]. Since the thermal budget in all devices was identical and the boron diffusion coefficient increases linearly with boron concentration [118], the collector current degradation should increase with boron doping. Device #458 doped 10^{19} cm^{-3} indeed had the biggest collector current improvement compared to the silicon control device #246 indicating that parasitic potential barriers were absent or small. Device #460 doped 10^{20} cm^{-3} without spacers had a similar E_A as the silicon control device because its collector current was controlled by the p-Si layers formed on both sides of the base by boron outdiffusion. The intrinsic $Si_{1-x}Ge_x$ spacer layers in device #457 doped 10^{20} cm^{-3} resulted in a 10× improved collector current compared to the device doped 10^{20} cm^{-3} without spacers. The ideal injection efficiency of device #458, however, was not recovered, possibly due to inadequate spacer thickness; nevertheless, this was the first demonstration of the performance improvement possible with intrinsic

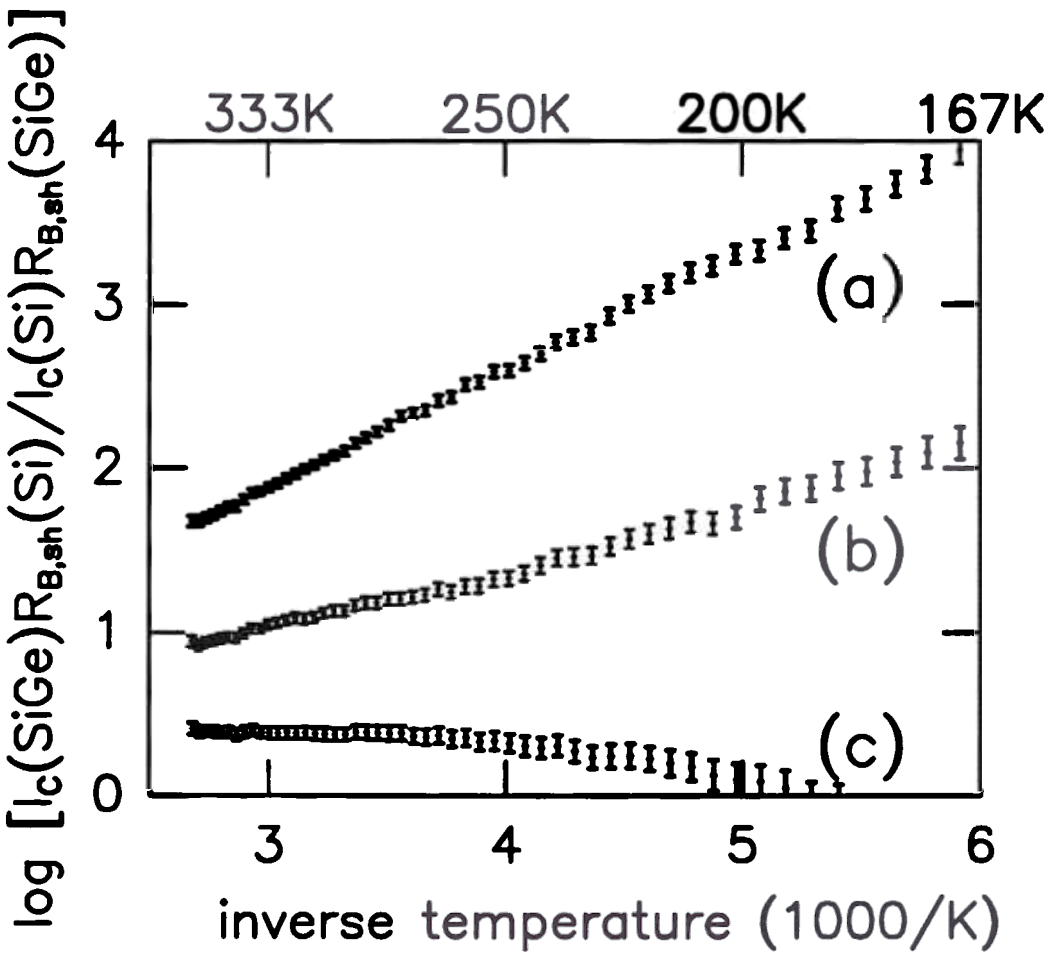


Figure 5.8: Measured collector current vs. inverse temperature for devices (a) #458, 5.5×10^{18} cm^{-3}, no spacers; (b) #457, 10^{20} cm^{-3}, 80 Å thick spacers; and (c) #460, 10^{20} cm^{-3}, no spacers, normalized to that of the silicon control device #246. This measurement proves the existence of a small parasitic barrier in device #457, and a large barrier in device #460.

$Si_{1-x}Ge_x$ layers in $Si/Si_{1-x}Ge_x/Si$ HBT's.

5.5 Analytical Model for Parasitic Barriers

In Section 4.4 an equation has been derived which allows to calculate the collector current of a HBT if the electrostatic potential $\Psi(x)$ is known in the base. Eqn. 4.12 demonstrates that the collector current is controlled by the region in the base where the conduction band presents the highest barrier for electrons.

In the case of base dopant outdiffusion three cases have to be considered, as shown in Figs. 5.1 and 5.5.

1. **no outdiffusion:** Both the Si and the $Si_{1-x}Ge_x$ side of the heterojunction are in a depletion region without forming a barrier to electron transport. The region presenting the highest barrier for electron flow is the charge-neutral base, and Kroemer's Eqn. 4.14 is valid (see Fig. 5.1 for an L_D of 0 Å).

2. **"flatband" case:** The $Si_{1-x}Ge_x$ side of the heterojunction is no longer depleted, but the Si side is still in a depletion region, as shown in Fig. 5.1 for an L_D of 11 Å. The highest barrier for electron flow is the small conduction band spike, but since at the $Si_{1-x}Ge_x/Si$ heterojunction $\Delta E_C \ll \Delta E_V$, the effect of the small conduction band spike on the collector current will barely be noticed.

3. **parasitic depleted barrier:** The $Si_{1-x}Ge_x$ side of the heterojunction is in an accumulation region, and the Si side in a depletion region forming a parasitic barrier in the conduction band (see Fig. 5.1 for an L_D of 33 Å). Since the parasitic barrier is fully contained in the combined depletion regions of the $Si_{1-x}Ge_x/Si$ heterojunction and the p-n junction, both its *height* and its *width* change with reverse bias V_{CB}. For calculating the collector current, the electrostatic potential has to be calculated explicitly and then input into Eqn. 4.12.

Kroemer's Eqn. 4.14 is not valid because the highest barrier seen by the electrons is not in the neutral base.

4. **charge-neutral barrier:** If the amount of dopant diffusing into the Si collector is sufficient to form a charge-neutral p-region separating the depletion regions of the $Si_{1-x}Ge_x$/Si heterojunction and the p-n junction, the collector current is controlled by the charge-neutral Si region and can be calculated using Kroemer's equation, Eqn. 4.14 (see Fig. 5.5(a) for $T = 900°C$).

We now focus on case (3.) of moderate outdiffusion resulting in a parasitic barrier which is fully contained in a depletion region. The potential $\Psi(x)$ in this case can be calculated for an exponentially decreasing base doping profile, shown in Fig. 5.1, by solving Poisson's equation in the fully depleted region between the n-collector and the $Si_{1-x}Ge_x$/Si heterojunction [119]:

$$N(x) = N_D \left(1 - e^{-\lambda(x-x_0)}\right)$$

where x_0 is the position of the p-n-junction. The boundary condition is that the potential difference $\Delta\Psi$ between the n-collector and the Si side of the $Si_{1-x}Ge_x$/Si heterojunction is the sum of the built-in potential V_{BI}, the applied base-collector reverse bias V_{CB}, and the voltage drop across the accumulation region ΔE_{ACC} at the $Si_{1-x}Ge_x$ side of the heterojunction:

$$\Delta\Psi = V_{BI} + V_{CB} + \Delta E_{ACC}$$

$$\Delta\Psi = E_G(Si) - \frac{k_B T}{q}\left(\ln\frac{N_C(Si)}{N_D} + \ln\frac{N_V(SiGe)}{N_A}\right)$$

$$- \Delta E_V + V_{CB} + \Delta E_{ACC}$$

Poisson's Equation in the depletion region between the $Si_{1-x}Ge_x$/Si heterojunction

and the collector is:

$$\frac{d^2\Psi}{dx^2} = \frac{q}{\epsilon_0\epsilon_{Si}} N_D \left(e^{-\lambda(x-x_0)} - 1\right) \tag{5.4}$$

and can be integrated with the boundary conditions $\Psi(W_C) = 0$ and $d\Psi/dx(W_C) = 0$. where W_C is the depletion region edge in the collector:

$$\Psi(x) = \frac{qN_D}{\epsilon_0\epsilon_{Si}} \left\{ \frac{e^{-\lambda(x-x_0)} - e^{-\lambda(W_C-x_0)}}{\lambda^2} + \frac{e^{-\lambda(W_C-x_0)}(x-W_C)}{\lambda} \right.$$
$$\left. \frac{x^2 - W_C^2}{2} + W_C(x-W_C) \right\}$$

If E_{ACC} were known, the correct value of W_C could be determined from the boundary conditions for Ψ. We start by *guessing* $\Delta E_{ACC} \approx 25$ meV, and calculate W_C such that the following boundary conditions are satisfied:

$$\Psi(W_C) = 0 \quad \text{and} \quad \Psi(L) = \Delta\Psi = V_{BI} + V_{CB} + \Delta E_{ACC}$$

where L is the position of the heterojunction. Then we calculate the values of the potential Ψ and the electric field $\mathcal{E} = -d\Psi/dx$ at the Si side of the heterojunction. The displacement vector $\mathcal{D} = \epsilon\epsilon_0\mathcal{E}$ is continuous at the heterojunction, so $\mathcal{E}$ on the $Si_{1-x}Ge_x$ side can be easily determined. Since the dielectric constant of the strained $Si_{1-x}Ge_x$ alloy has not yet been determined, we interpolate between the values of pure silicon and pure germanium, as suggested in Ref. [108]:

$$\epsilon_{SiGe} = \frac{1 + 2\left[\, x\,(\epsilon_{Ge}-1)/(\epsilon_{Ge}+2) + \,(1-x)\,(\epsilon_{Si}-1)/(\epsilon_{Si}+2)\right]}{1 - \,x\,(\epsilon_{Ge}-1)/(\epsilon_{Ge}+2) - \,(1-x)\,(\epsilon_{Si}-1)/(\epsilon_{Si}+2)}$$

$$\mathcal{E}(SiGe) = \mathcal{E}(Si)\,\frac{\epsilon_{Si}}{\epsilon_{SiGe}}$$

From $\mathcal{E}(SiGe)$ the potential drop ΔE_{ACC} across the accumulation layer of the heterojunction can be calculated [120]:

$$\mathcal{E} = \frac{\sqrt{2}k_BT}{qL_D}\sqrt{e^{q\Delta E_{ACC}/k_BT} - \frac{q\Delta E_{ACC}}{k_BT} - 1} \tag{5.8}$$

$$L_D = \sqrt{\frac{\epsilon_0 \epsilon_{SiGe} k_B T}{q^2 N_A}}$$

L_D is the extrinsic Debye length for holes. We now insert ΔE_{ACC} into Eqn. 5.3 and iterate until ΔE_{ACC} has converged. This usually takes only one or two steps.

calculated potential $\Psi(x)$ can now be inserted into Eqn. 4.12 to obtain the collector current which is controlled by the parasitic barrier. The integral in the denominator of Eqn. 4.12 can be simplified by approximating the parasitic barrier by a parabola located at L_0 where the conduction band E_C has its maximum value, or $\Psi = (-E_C(Si) + \chi(Si) + const.)$ has its minimum value:

$$\frac{1}{\lambda}\left(e^{-\lambda(L_0 - x_0)} - e^{-\lambda(W_C - x_0)}\right) - W_C + L_0 = 0 \tag{5.9}$$

Then $\Psi(x)$ is expanded into a Taylor series around L_0, which is truncated after the quadratic term and input into the exponential in the denominator of Eqn. 4.12. The limits of the integral are expanded from $-\infty$ to ∞, which yields the contribution of the parasitic barrier to the effective Gummel number in terms of a potential minimum $\Psi(L_0)$ and an *effective* barrier width Σ_B

$$\Sigma_B = \sqrt{\frac{2\pi k_B T}{q}\left(\left.\frac{d^2\Psi}{dx^2}\right|_{x=L_0}\right)^{-1}} \tag{5.10}$$

Finally, Eqn. 4.12 is simplified to:

$$J_C = -\frac{q\left[\exp\left(qV_{BE}/k_BT\right) - \exp\left(qV_{BC}/k_BT\right)\right]}{\int_{neutral\ base} \frac{N_A(x)}{D_n(x)\, n_i^2(x)}\, dx + \frac{\Sigma_B}{D_n(L_0) N_C(L_0)}\, e^{-q\Psi(L_0)/k_BT}} \tag{5.11}$$

A comparison between the calculated conduction band using the analytical model and the numerical simulation of Section 5.2 is shown in Fig. 5.9 for the device of Fig. 5.1 with an L_D of 22 Å. Good agreement is obtained.

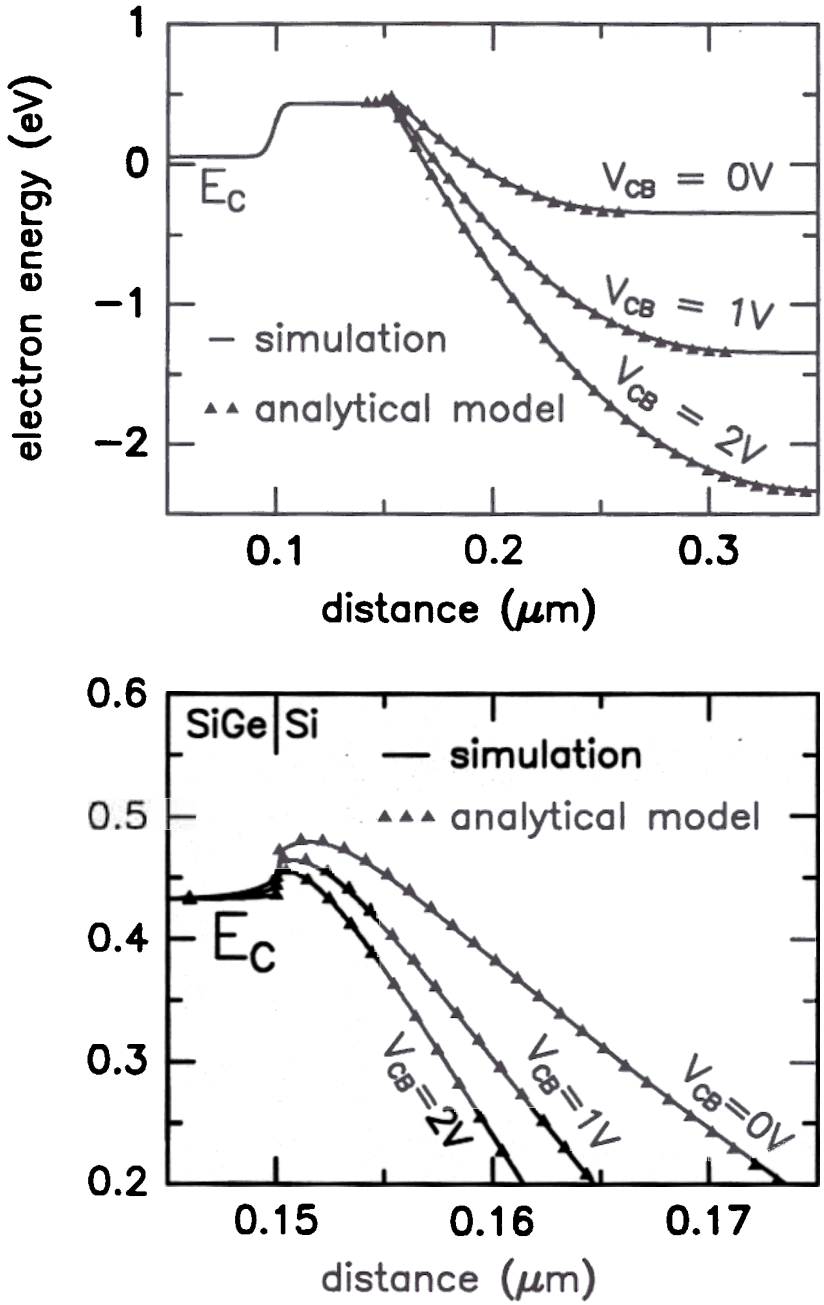


Figure 5.9: Comparison of analytical model and numerical simulation for the conduction band of a device with an exponential boron outdiffusion tail from the p-$Si_{1-x}Ge_x$ base into the collector (L_D = 22 Å). Note that both the *height* and the *width* of the barrier depends on the applied base-collector reverse bias.

Chapter 6

The Current Gain-Early Voltage Tradeoff in Graded Base HBT's

6.1 Introduction

The trade-off between common-emitter current gain β and Early voltage V_A is important for analog applications of bipolar transistors. The two parameters β and V_A are related to the common-emitter current gain and the output resistance of the transistor, as shown in the small signal model of Fig. 6.1. In this model, the output of the transistor is represented by a current source βI_B in parallel with an output resistance $r_O = V_A/I_C$. The βV_A product is a figure of merit for analog applications of bipolar transistors; the output resistance R_O of the cascode amplifier, which is commonly used in current sources, for example, is proportional to the βV_A product.

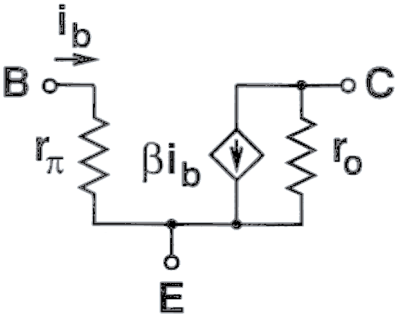


Figure 6.1: Small signal model of a bipolar transistor. The output is represented by a current source βI_B in parallel with an output resistance $r_O = V_A/I_C$.

The Early voltage V_A which characterizes the output resistance of a bipolar transistor is usually defined from the common-emitter $I_C(V_{CE};\ I_B = const.)$ characteristic of the device as shown in Fig. 6.2. Plotted are curves of I_C vs. V_{CE} for constant base current steps. In the active region of operation the base-collector junction is reverse biased ($V_{CE} \geq V_{BE}$, or $V_{CB} \geq 0$ V) and the collector current increases with the reverse bias of the base-collector junction. It is usually observed that the tangents to the linear regions of the output characteristics at zero base-collector reverse bias extrapolate to a constant voltage V_A for zero collector current. V_A is called *Early voltage*. From Fig. 6.2 the definition of V_A can be readily obtained:

$$V_A = I_C \frac{\partial V_{CE}}{\partial I_C} - V_{CE}\Big|_{I_B=const} \approx I_C \frac{\partial V_{CB}}{\partial I_C} \tag{6.1}$$

For analog applications of bipolar transistors, a high value of V_A is desired.

There are several physical effects which can cause the collector current I_C to increase with collector-emitter voltage for constant base current. The most important effect in homojunction devices is the Early effect, the increase of the collector current caused by a decrease of the width of the neutral base with base-collector reverse bias

In this chapter we present for the first time a simple analytical model for the tradeoff between β and V_A in graded-base HBT's, and show that high values of βV_A can be obtained in $Si/Si_{1-x}Ge_x/Si$ HBT's without critical thickness problems.

Analytical Model for β vs. V_A Tradeoff in Graded-Base HBT's

A simple analytical model for the tradeoff between β and V_A in HBT's with arbitrary base doping and bandgap profiles can be developed based on charge-control theory [104, 105]. Two cases have to be considered in analogy to the derivation of the collector current of Section 4.4. We first investigate the case of a charge neutral base

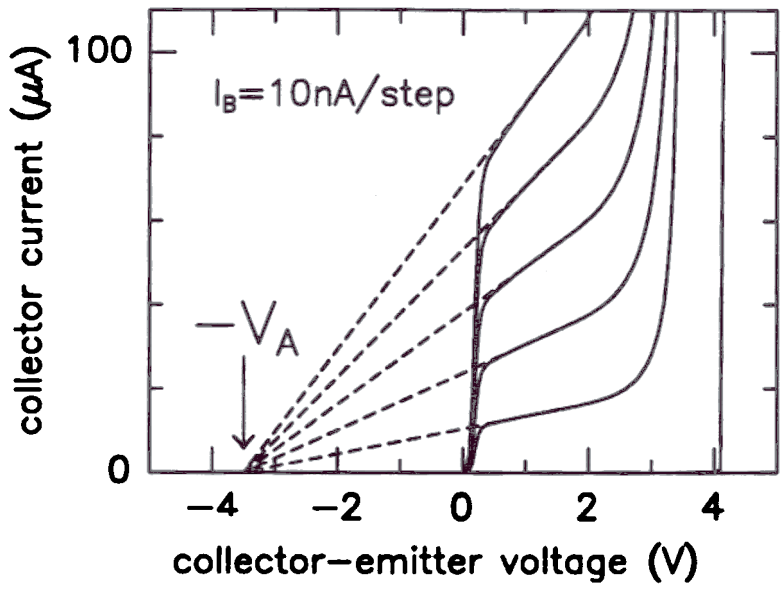


Figure 6.2: Definition of the Early voltage V_A. The linear parts of the output characteristics (collector current vs. collector-emitter voltage for constant base current steps) of a bipolar transistor are extrapolated to zero collector current.

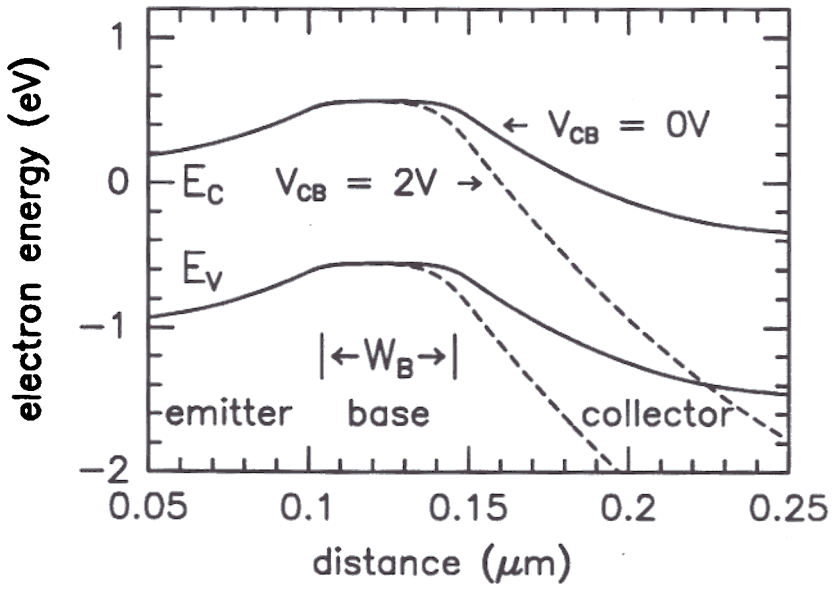


Figure 6.3: Band diagram of a bipolar transistor showing the Early effect. Applying a reverse bias at the collector terminal decreases the width of the neutral base resulting in increased collector current.

region starting with Kroemer's Eqn. 4.14. Then, in Section 6.5, we discuss the more general case with depleted barriers in the base

If there is no fully depleted parasitic barrier at the base-collector junction, the β vs. V_A tradeoff can be calculated from Kroemer's equation for the collector current in a HBT with nonuniform bandgap in the base [106]. Starting from Eqn. 4.14, the current gain β is calculated assuming that the base current is controlled by hole injection into the emitter (see Eqn. 2.3):

$$J_B = J_{B,0}\, e^{qV_{BE}/k_BT}$$

where $J_{B,0}$ is *independent* of the base doping and bandgap profiles. Then the Early voltage is calculated from Eqn. 6.1 assuming that the width of the neutral base W_B changes with reverse bias V_{CB} as in

$$\frac{\partial W_B}{\partial V_{CB}} = -\frac{C_{BC}(V_{CB})}{qN_A(W_B)}.$$

Since in a typical bipolar transistor the collector doping is much smaller than the base doping, C_{BC} is determined by the collector doping profile. The resulting equations for β and V_A describe the β vs. V_A tradeoff in HBT's where the bandgap can vary in the base:

$$\beta \simeq \frac{J_C}{J_B} = \frac{q}{J_{B,0}} \left(\int_{base} \frac{N_A(x)}{n_i^2(x) D_n(x)}\, dx \right)^{-1}$$

$$V_A = J_C \frac{\partial V_{CB}}{\partial J_C} = \frac{q}{C_{BC}(V_{CB})} \left[n_i^2 D_n \right]_{x=W_B} \left(\int_{base} \frac{N_A(x)}{n_i^2(x) D_n(x)}\, dx \right)$$

where the integral is taken over the neutral base. Since n_i^2 depends exponentially on the bandgap of the semiconductor material, the integral in brackets (the generalized Gummel number) will be dominated by the region with the smallest n_i^2, i.e. the largest bandgap. The current gain, therefore, depends most significantly on the largest bandgap in the base V_A is determined by the ratio of n_i^2 at the edge of the

base-collector depletion region in the base (W_B) and the smallest n_i^2 in the base, corresponding exponentially to the difference between the widest energy gap in the base and the energy gap at the edge of the base-collector depletion region in the base, divided by k_BT. The βV_A product, however, is independent of the actual base profile and depends to first order only on n_i^2 (or exponentially on the the bandgap) at the collector edge of the base

$$\beta V_A = \frac{q^2}{J_{B,0} C_{BC}(V_{CB})} \left[n_i^2 D_n \right]_{x=W_B} \tag{6.6}$$

Eqns. 6.4 and 6.5 will now be applied for some special cases.

Si Homojunction Devices with Arbitrary Base Doping Profiles

In this case the intrinsic carrier concentration is constant in the base:

$$\beta = \frac{J_C}{J_B} = \frac{q n_i^2}{J_{B,0}} \left(\int_{base} \frac{N_A(x)}{D_n(x)} \, dx \right)^{-1} \tag{6.7}$$

$$V_A = J_C \frac{\partial V_{CB}}{\partial J_C} = \frac{q}{C_{BC}} \left[D_n \right]_{x=W_B} \left(\int_{base} \frac{N_A(x)}{D_n(x)} \, dx \right) \tag{6.8}$$

Note that the βV_A product in homojunction transistors does not depend on the doping distribution in the base, indicating that grading the base doping concentration does not increase the βV_A product

6.2.2 Flat-Base $Si/Si_{1-x}Ge_x/Si$ HBT's

Again, the intrinsic carrier concentration is constant throughout the base. Compared with a Si homojunction device, βV_A is exponentially increased by the bandgap reduction ΔE_G:

$$\beta = \frac{J_C}{J_B} = \frac{q n_i^2(Si) N_C N_V(SiGe)}{J_{B,0} N_C N_V(Si)} \left(\int_{base} \frac{N_A(x)}{D_n(x)} \, dx \right)^{-1} e^{\Delta E_G / k_B T} \tag{6.9}$$

$$V_A = J_C \frac{\partial V_{CB}}{\partial J_C} = \frac{q}{C_{BC}(V_{CB})} \left[D_n \right]_{x=W_B} \left(\int_{base} \frac{N_A(x)}{D_n(x)} \, dx \right) \tag{6.10}$$

The flat-base $Si/Si_{1-x}Ge_x/Si$ HBT has an exponentially increased current gain, but approximately the same Early voltage as a homojunction transistor with the same base doping profile. As described in Chap. 2.3, the current gain in the flat-base HBT can be traded for a lower base sheet resistance by increasing the base doping. This also increases the Early voltage, which is well-known in III/V HBT's where Early voltages of more than 100 V can be achieved in devices with narrow, heavily doped bases [122]. The increase in β results in an improvement of the βV_A product by a factor of $\exp(\Delta E_G/k_BT)$ compared to homojunction devices.

In $Si/Si_{1-x}Ge_x/Si$ flat base HBT's the improvement in βV_A is limited by critical thickness considerations. Although it is possible to exceed the equilibrium critical thickness in fully strained $Si_{1-x}Ge_x$ layers, the films in this metastable state have the tendency to relax by incorporating misfit dislocations upon exposure to temperatures typical of integrated circuit processing. This puts a limit to the integrated Ge content in the base, and therefore to the bandgap difference between emitter and base in a flat base HBT. For example, for a base width of about 500 Å, the Matthews-Blakeslee theory predicts a maximum Ge concentration of about 7% corresponding to a bandgap difference of 60 meV compared to Si, as shown in Fig. 6.4. This bandgap difference translates into an $\approx 5\times$ improvement in the βV_A product if the strain-induced reduction of $N_C N_V$ described in Sec. 4.5 is taken into account.

6.2.3 Graded Bandgap Base HBT's

The Early effect in graded base HBT's can be qualitatively understood by considering the shape of the conduction band in the base. The collector current consists of electrons being injected from the emitter into the base. It is controlled by the region in the base with the highest barrier in the conduction band with respect to the Fermi level corresponding to the region with the widest bandgap and the heaviest doping. The Early voltage depends on the change in the width of the highest barrier in the

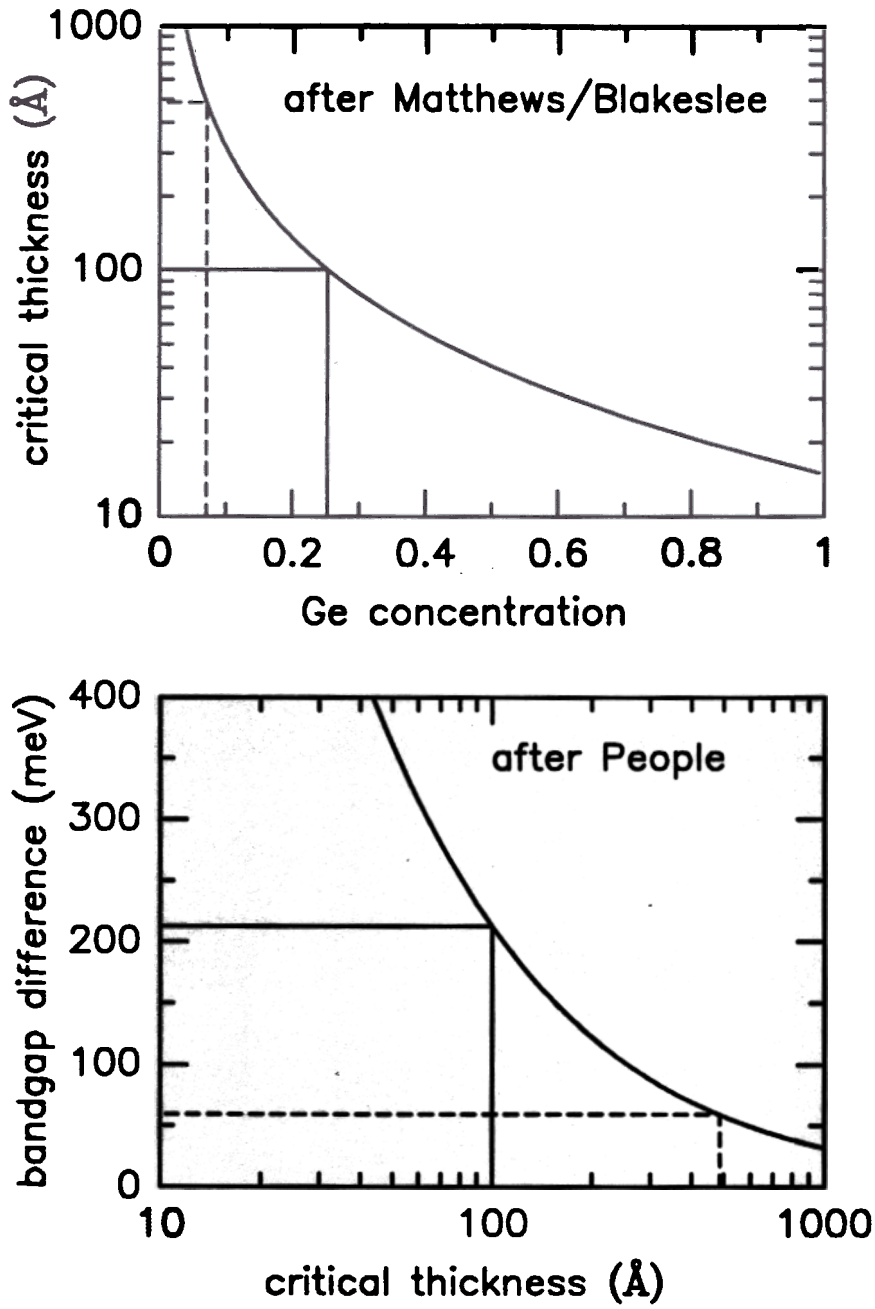


Figure 6.4: Critical thickness limitation in $Si/Si_{1-x}Ge_x/Si$ HBT's showing that thin $Si_{1-x}Ge_x$ layers are preferred, because a big bandgap difference ΔE_G can be obtained without exceeding the equilibrium critical thickness.

base with base-collector reverse bias. If the highest barrier for electrons in the base is at the *base-emitter* junction, increasing the base-collector reverse bias has little effect on the shape of this barrier resulting in a large Early voltage. This situation corresponds to a device with a narrow gap region near the collector like the linearly graded base devices of Chap. 4. Conversely, if the highest barrier for electrons is at the *base-collector* junction, even a small change in V_{CB} changes the width of this highest barrier resulting in increased collector current, and a low Early voltage.

This indicates that inserting a very thin $Si_{1-x}Ge_x$ region close to the collector would increase the Early voltage dramatically while leaving the current gain approximately unchanged, resulting in a vast improvement in βV_A. The thickness of the $Si_{1-x}Ge_x$ layer at the collector has to be sufficient to include the base edge of the base-collector depletion region even at maximum reverse bias V_{CB}. Since the equilibrium critical thickness decreases with increasing Ge concentration in a strained $Si_{1-x}Ge_x$ layer, the improvement possible in the βV_A product of a graded-base HBT is bigger compared to that of β alone in a flat-base HBT, because even a thin $Si_{1-x}Ge_x$ layer at the collector side of the base results in a high βV_A product wherease a thick $Si_{1-x}Ge_x$ layer (the whole neutral base) is required to improve β alone. Fig. 6.4 shows that a 100 Å thick $Si_{1-x}Ge_x$ layer is thermodynamically stable up to a Ge concentration of 25% corresponding to a bandgap difference of 210 meV compared to silicon, and to a 1200× improvement in βV_A

The simplest structure to investigate the β vs. V_A tradeoff in graded base HBT's is a stepped-base transistor where the base consists of two p-doped layers with constant bandgap in each layer (see for example Fig. 6.5). In this structure the bandgap at the edge of the base-collector depletion region is independent of base-collector reverse bias which facilitates the comparison between measured parameters and analytical modeling. Note that in an HBT with linearly graded bandgap in the base, the bandgap at the edge of the base-collector depletion region depends on the base-collector reverse

Electrical Measurements on Stepped-Base and Flat-Base HBT's

For this experiment, both stepped-base and flat-base devices were fabricated with the process described in Chap. 3. All devices had identical emitter and collector layers. The bases consisted of two nominally 200 Å thick $Si_{1-x}Ge_x$ layers with constant Ge profile and boron doping of about 10^{18} cm^{-3}, as shown in Table 6.1. On both sides of the base, nominally 40 Å thick intrinsic $Si_{1-x}Ge_x$ spacer layers were inserted to remove spike-and-notch and outdiffusion effects which will be described in Section 6.5. The base currents of all devices had ideality factors between 1.0 and 1.2 with a $J_{B,0}$ of about 4 pA/cm^2, except device #641(I) with a $J_{B,0}$ of 10 pA/cm^2 leading to a smaller gain than expected. It is believed that in this device the 500 Å thick base with 25% Ge relieved strain by incorporating misfit dislocations which degraded its base current.

Table 6.1 lists results of electrical measurements performed to compare measured values of β and V_A to the simple theory outlined below. For all wafers, the pinched base sheet resistance $R_{B,sh}$ was measured on Hall bars which were given the same processing as the transistors, except that they did not receive the emitter implant. Device #642(H) had the highest $R_{B,sh}$ indicating that the growth rate at 625°C was lower than expected. The breakdown voltages BV_{CEO} (base terminal floating) and BV_{CBO} (emitter terminal floating) which should depend only on the collector doping profile were similar in all devices. The collector doping profiles were determined from capacitance-voltage measurements at 100 kHz where a DC reverse bias was applied to the collector while emitter and base were grounded. At a reverse bias of 0.5 V all devices had a base-collector capacitance of about 55 nF/cm^2. The current gains and

Table 6.1: Measured and calculated parameters of stepped-base and flat-base HBT's showing the β vs. V_A tradeoff in $Si/Si_{1-x}Ge_x/Si$ HBT's. The base-collector capacitance C_{BC} and the Early voltage V_A were measured at $V_{CB} = 0.5$ V.

device	642(H)	640(G)	637(F)	641(I)
%Ge at emitter	14	25	14	25
%Ge at collector	14	14	25	25
$R_{B,sh}$ (k$\Omega/\square$)	13.2	9.7	7.1	6.0
BV_{CEO} (V)	4.7	4.1	4.5	3.8
BV_{CBO} (V)	14.9	16.3	16.0	15.3
$J_{B,0}$ (pA/cm^2)	3.7	3.9	4.9	10.0
C_{BC} (nF/cm^2)	55	54	54	55
forward β	750	1800	1400	1750
forward V_A (V)	18	6	120	44
forward βV_A (V)	13500	10800	168000	77000
calculated βV_A (V)	10700	8980	190000	84000
reverse V_A (V)	13	100	3.5	42

Early voltages of Table 6.1 were determined at a base-collector reverse bias of 0.5 V from collector current measurements as shown in Fig. 6.2.

Fig. 6.5 shows calculated band diagrams and measured collector current characteristics for the stepped-base devices #640(G) and #637(F). Both devices had similar current gains because of the similar width and height of the highest barrier for electrons in the base. The output resistance of device #637(F) in which the narrow-gap layer was located at the base-collector junction, however, was vastly increased compared to device #640(G) which had its narrow-gap layer at the base-emitter junction. To prove that the location of the biggest barrier for electrons in the base is crucial for the Early voltage, collector current measurements were also taken in reverse mode, i.e. emitter down. As shown in Fig. 6.6, the relative performance of devices #640(G)

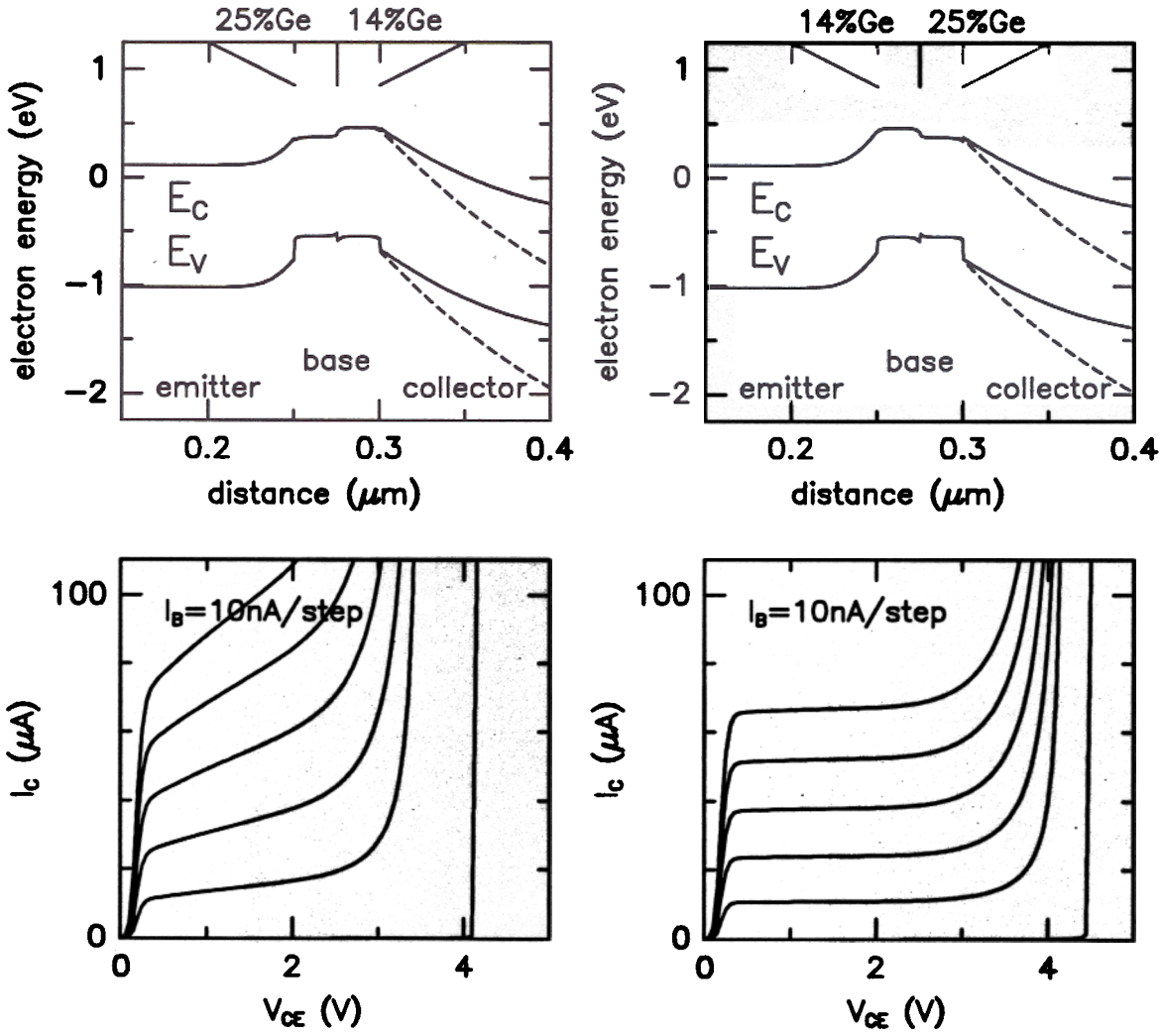


Figure 6.5: Calculated band diagrams and measured collector current characteristics showing the effect of the position of the biggest bandgap region in the base on the output resistance of HBT's (left: device #640(G); right: device #637(F)). Both devices had an emitter area of 62×62 μm^2.

and #637(F) was reversed. Although the base currents were nonideal because of the mesa-isolation, device #640(G) indeed had the highest Early voltage compared to devices #642(H) and #637(F). These results prove for the first time the concept that high Early voltages can be achieved by base profile engineering.

6.4 Comparison of Analytical Model and Experiment

With the measured values of C_{BC} and $J_{B,0}$ Eqn. 6.6 can be compared to the experimentally obtained values of β and V_A of the devices of Table 6.1, as shown in Fig. 6.7. Since the minority carrier diffusion coefficient D_n in $Si_{1-x}Ge_x$ perpendicular to the growth plane has not yet been determined, it was assumed to be identical to the value for silicon measured by Swirhun *et al.* [79]. The bandgap reduction in the strained $Si_{1-x}Ge_x$ layer was taken from People's calculation [30]. The reduction of the effective densities of states caused by the strain was taken into account as in Chap. 4.5. The model, which has no adjustable parameters, fits the experimental data well. To put these results into perspective, Fig. 6.8 shows the βV_A product vs. cutoff frequency f_T for state-of-the-art silicon bipolar transistor processes used in analog applications [123]. Note that in general the βV_A product decreases with increasing f_T because of the increased collector doping (and base-collector capacitance) necessary to allow the devices to operate at high current levels without base pushout (Kirk effect, [114]). For device #637(F), the cutoff frequency f_T is expected to be on the order of 30 GHz based on published results of comparable device structures with similar f_T [73]. This indicates a $\times 100$ improvement in βV_A over the state-of-the-art, as shown in Fig. 6.8, and shows the enormous potential of $Si/Si_{1-x}Ge_x/Si$ HBT's for analog applications.

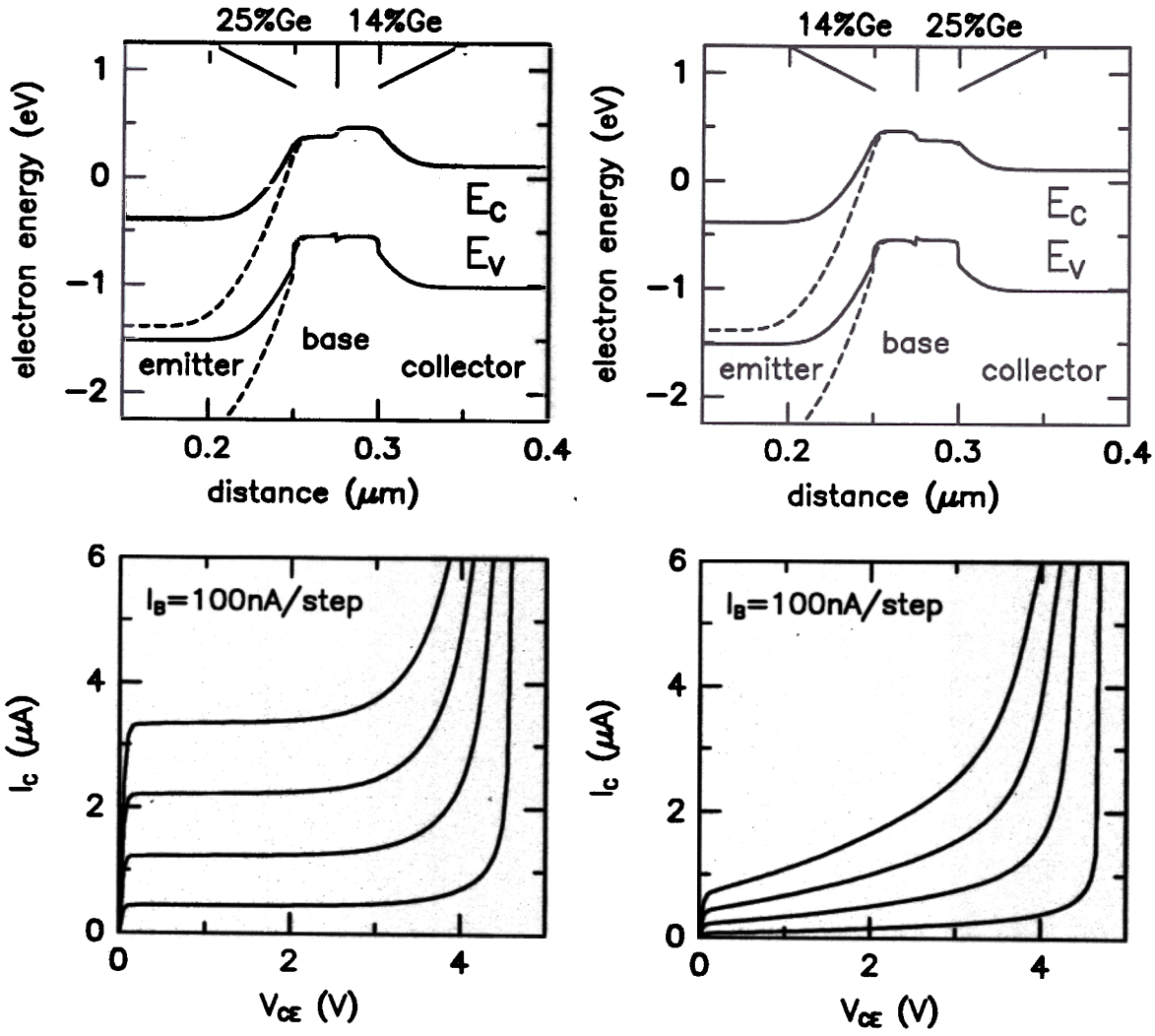


Figure 6.6: Calculated band diagrams and measured collector current characteristics in "collector-up" configuration (left: device #640(G); right: device #637(F)).

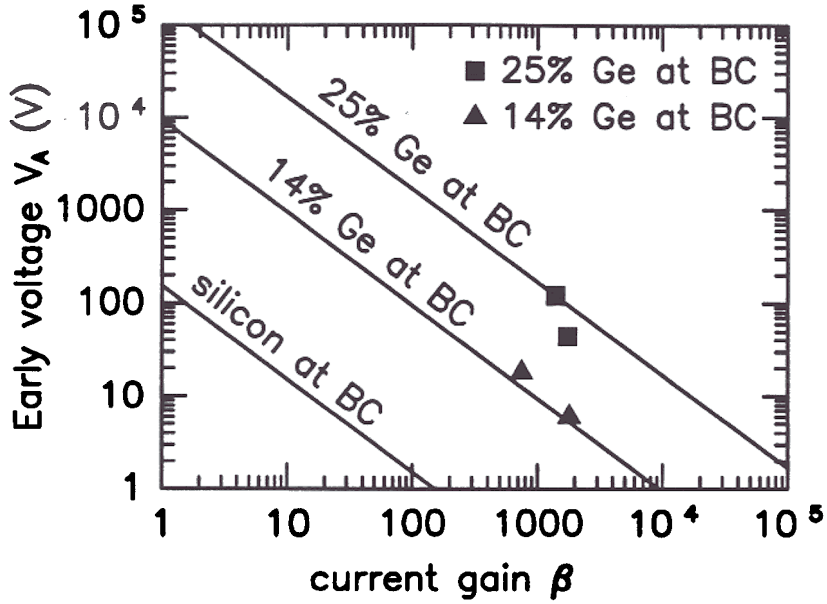


Figure 6.7: β vs. V_A tradeoff in $Si/Si_{1-x}Ge_x/Si$ HBT's. Shown are calculated lines of constant βV_A product for various Ge concentrations *at the base-collector junction* and experimental values for both flat-base and stepped-base HBT's

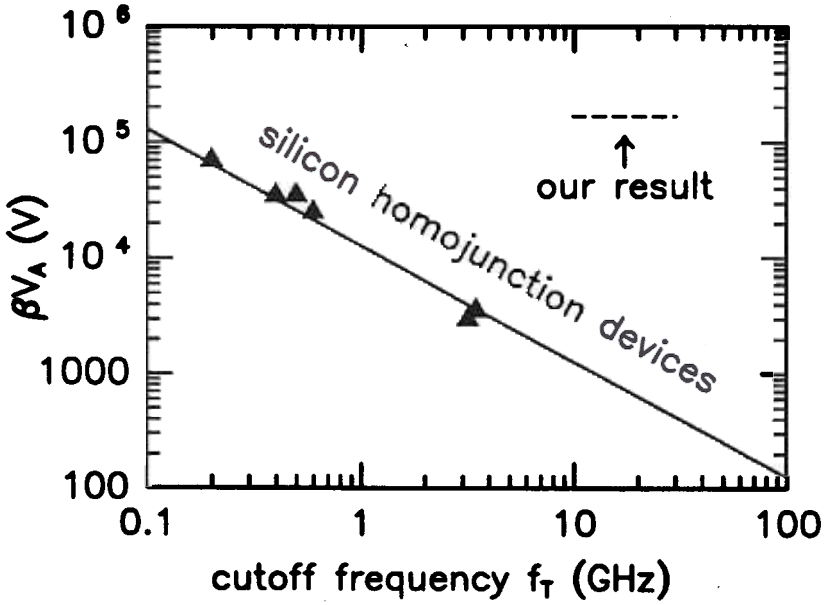


Figure 6.8: βV_A product vs. cutoff frequency f_T for all-silicon analog bipolar processes. For comparison, the experimentally obtained value for device #637(F) is shown with an estimated range for f_T based on published results of comparable devices.

6.5 Early Voltage Degradation by Base Dopant Outdiffusion

In Chap. 5 it was shown that non-abrupt doping profiles can cause parasitic potential barriers in the conduction band of a HBT which decrease the current gain. In this section we shall demonstrate that even small amounts of dopant outdiffusion degrade the Early voltage enormously, if the parasitic barriers are fully contained in a depletion region (case 3 of Section 5.5), because both their *height* and *width* change with base-collector reverse bias, and the collector current is exponentially dependent on the height of the parasitic barriers. This is evident from Eqn. 5.11, because the highest potential barrier dominates the denominator, and can also be seen from the simulated band diagram of Fig. 5.9 of the device of Fig. 5.1 with an L_D of 22 Å.

The simulated J_C vs. V_{CB} curves from Fig. 6.9 show that an L_D of 22 Å reduces the collector current at zero base-collector bias by about 30%. The Early voltage, however, is much more strongly affected, as shown in the V_A vs. V_{CB} curves of Fig. 6.10 calculated from Fig. 6.9. For an L_D of 22 Å, V_A is decreased by more than 10× compared to an "ideal" device with 50 Å thick spacers. For this reason, the 40 Å thick spacers were inserted into the stepped-base devices of Section 6.3.

We now present electrical measurements of device #636 with a $Si_{0.86}Ge_{0.14}$ flat base ($R_{B,sh}$ = 3500 Ω/□) and thin spacers, and prove that a small amount of base dopant outdiffusion has degraded its Early voltage. Fig. 6.11 shows its common-emitter characteristics. The output resistance depends strongly on output voltage, which is apparent from Fig. 6.12 showing the Early voltage calculated from the data of Fig. 6.11 with Eqn. 6.1.

There are several possible causes for a strong dependence of the output resistance r_O on the output voltage V_{CE}. Since the Early voltage is inversely proportional to the base-collector capacitance and C_{BC} decreases with reverse bias V_{CB}, the collector

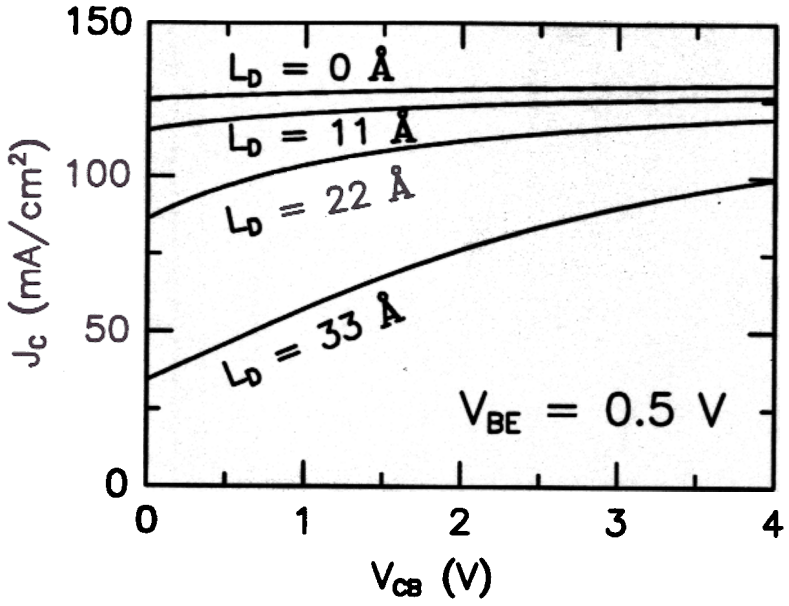


Figure 6.9: Simulated collector current density at a temperature of 293 K and a base-emitter bias of $V_{BE} = 0.5$ V of a device with a 500 Å wide $Si_{0.80}Ge_{0.20}$ base doped 10^{19} cm^{-3}, and a collector doping of 10^{17} cm^{-3}, for various values of L_D.

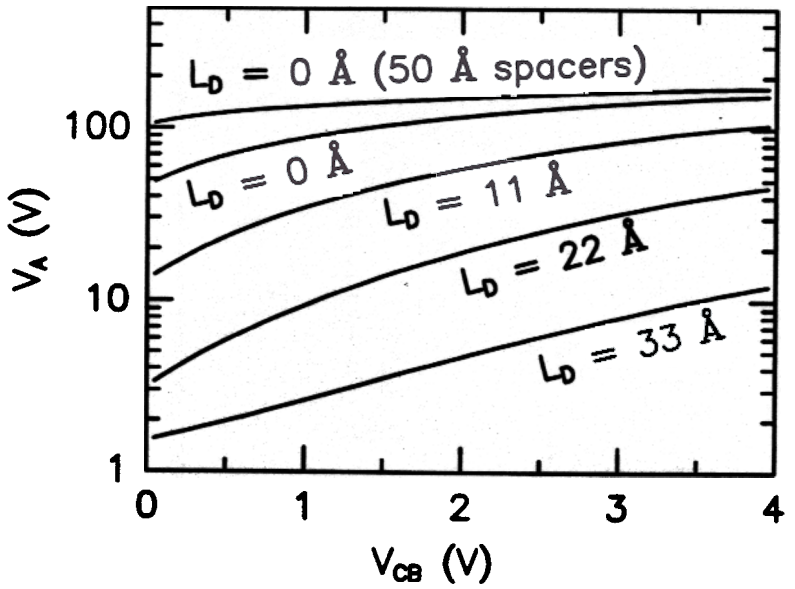


Figure 6.10: Early voltage calculated from the simulated J_C vs. V_{CB} curves. Compared to the "ideal" device with spacers, in the device with no dopant outdiffusion where the $Si_{1-x}Ge_x$/Si interfaces coincide with the doping interfaces, V_A decreases slightly because of the conduction band spike ΔE_C at the heterojunction. Even small amounts of dopant outdiffusion, however, cause a much stronger V_A degradation.

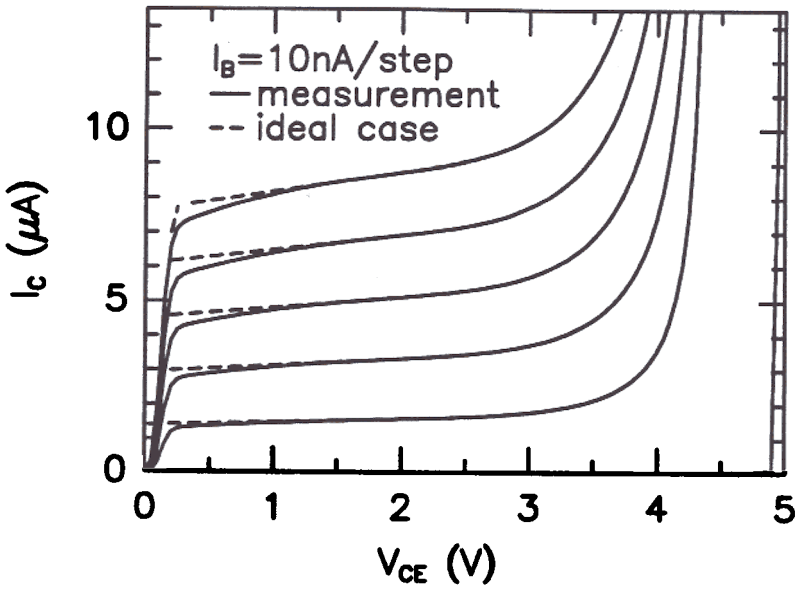


Figure 6.11: Measured collector current characteristics of device #636 with a base doped about 10^{19} cm^{-3} and small spacers (solid lines); and expected ideal behavior (dashed lines) for comparison. Note that the output resistance depended strongly on the output voltage indicating the presence of a parasitic barrier in the conduction band at the base-collector junction

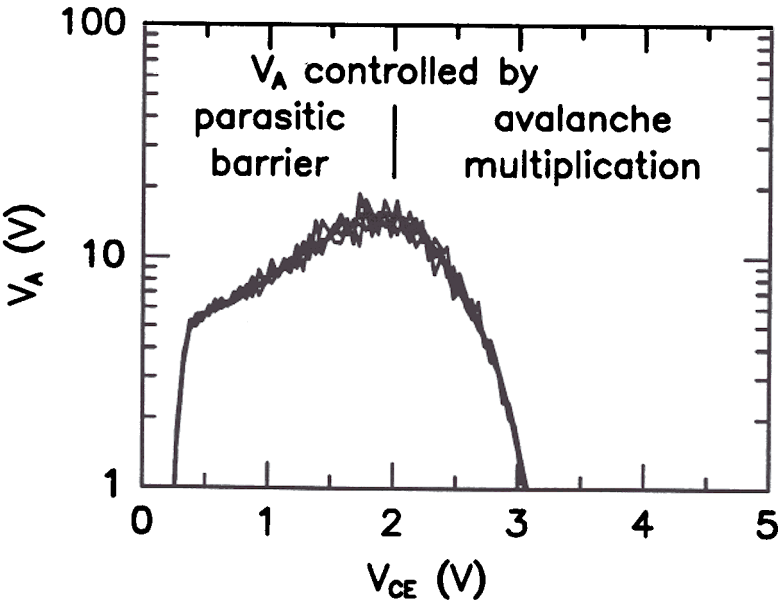


Figure 6.12: Early voltage calculated from the above common-emitter characteristics. For $V_{CE} \leq 2$ V the Early voltage was controlled by the parasitic barrier at the base-collector junction, while for $V_{CE} \geq 2$ V avalanche multiplication limited V_A.

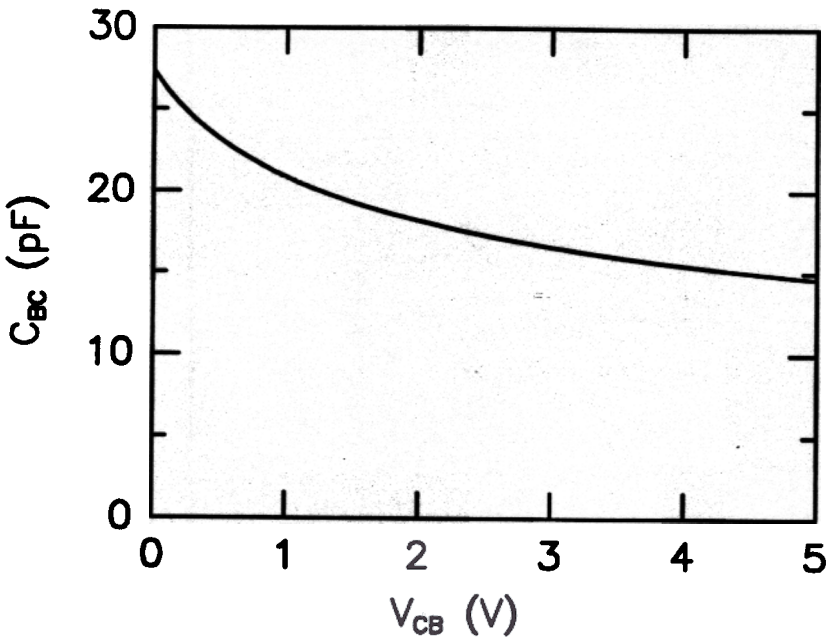


Figure 6.13: Base-collector capacitance C_{BC} vs. base-collector reverse bias V_{CB} of device #636 measured at a frequency of 100 kHz.

design influences the output resistance. Fig. 6.13 shows the measured base-collector capacitance vs. base-collector reverse bias. The 33% reduction in C_{BC} between V_{CB} = 0 V and V_{CB} = 2 V was not sufficient to explain the much stronger Early voltage degradation.

If the Early voltage is determined from $I_C(V_{CE}, I_B = const.)$ measurements as shown in Fig. 6.2, it could also be degraded by a change of the distribution of the current going into the base terminal among the various base current components described in Section 2.2. This is because a common-emitter $I_C(V_{CE}, I_B = const.)$ measurement determines the collector current *not* for a constant forward bias V_{BE}, but it determines β vs. V_{CE} for a constant I_B. To determine whether the Early voltage is degraded by changes in the base or the collector current, it is necessary to measure the relative changes of I_B and I_C as a function of V_{CE} at a constant V_{BE}. The Early

voltage measured in a common-emitter configuration, which is the relative change in β with V_{CE}, is then related to the relative changes of the base and collector currents by:

$$\frac{1}{\beta}\frac{\partial\beta}{\partial V_{CE}} = \frac{1}{I_C}\frac{\partial I_C}{\partial V_{CB}} - \frac{1}{I_B}\frac{\partial I_B}{\partial V_{CB}} \tag{6.11}$$

$$\frac{1}{V_{A,C}} \equiv \frac{1}{I_C}\frac{\partial I_C}{\partial V_{CB}} \quad \text{and} \quad \frac{1}{V_{A,B}} \equiv \frac{1}{I_B}\frac{\partial I_B}{\partial V_{CB}} \quad \Longrightarrow \quad \frac{1}{\beta} = \frac{1}{V_{A,C}} + \frac{1}{V_{A,B}} \tag{6.12}$$

In conventional homojunction transistors the Early voltage is dominated by the Early effect, i.e. by a relative change in I_C with V_{CB}. In $Si/Si_{1-x}Ge_x/Si$ HBT's or advanced bipolar transistors, however, changes in the base current with V_{CB} can degrade the output resistance. For example, increasing the base-collector reverse bias V_{CB} reduces the width of the neutral base, reducing the base current if it is dominated by neutral base recombination (note that J_S in Eqn. 2.4 is proportional to the width of the neutral base). Since in device #636 the base current was similar to the one of a silicon control device indicating that it was dominated by hole injection into the emitter, we conclude that neutral base recombination did not cause the observed V_A degradation.

Increasing V_{CB} also causes electron-hole generation in the base-collector depletion region by thermal generation or avalanche effect. The electrons contribute to the collector current, and the holes are swept into the base adding to the externally injected base current. Since $I_C \quad \beta I_B$, and the electron and hole current components due to avalanche effect (ΔI_C and ΔI_B) are equal, the effect of the base current increase on current gain is much bigger than the effect of the collector current increase. Avalanche effect limits the breakdown voltage BV_{CEO} in transistors with heavily doped collectors (i.e. $N_A \approx 10^{17}$ cm^{-3}) because of the high electric fields in the base-collector depletion region; it can be minimized by a reduced-field design in the collector as described in Ref. [124]

To determine the onset of weak avalanche multiplication, collector and base currents were measured at constant base-emitter bias V_{BE} (see Figs. 6.14–6.17), which independently demonstrated the effect of changes in I_B and I_C on the common-emitter current gain β. From the measured curves of base current I_B vs. base-collector bias V_{CB} for constant base-emitter bias V_{BE} it was apparent that at a reverse bias V_{CB} of about 3.8 V the externally measured base current changed its polarity, a phenomenon called "bipolar snap-back" (see Fig. 6.14) [125]. Weak avalanche multiplication in the collector degraded the output resistance even at values of V_{CB} as low as 1.6 V, as can be seen from Fig. 6.15, where the contribution of the base current to the Early voltage is plotted vs. V_{CB}.

The Early effect can be observed from the measured collector current vs. V_{CB} curves (see Fig. 6.16). At values of V_{CB} below 3.8 V avalanche current can be neglected because from Fig. 6.14 can be seen that it was smaller than the base current (and $I_B \ll I_C$). The contribution of the relative change of the collector current with V_{CB} to the Early voltage is shown in Fig. 6.17. This measurement proved that the Early voltage degradation at low values of V_{CB} seen in Fig. 6.11 was indeed due to a change in the collector current; since the increase in $V_{A,C}$ with V_{CB} was much bigger than the corresponding decrease in C_{BC} from Fig. 6.13, we conclude that small amounts of dopant outdiffusion degraded the collector current.

The formation of parasitic barriers in the conduction band, demonstrated here for the first time by simulations, an analytical model, and electrical measurements, mandates that dopant outdiffusion from the $Si_{1-x}Ge_x$ base into the silicon collector cannot be tolerated in analog applications of $Si/Si_{1-x}Ge_x/Si$ HBT's. Intrinsic $Si_{1-x}Ge_x$ spacer layers on both sides of the base should be considered according to the thermal budget of the process, as discussed in Chap. 5.3.